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Scala_15L

CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : Scala-15L
PBA Name : MAIN
PCB Code : GCE : BA41-01378A
 : NAN : BA41-01377A
 : HAN : BA41-01379A
 : GBM : BA41-01380A
Dev. Step : PV
Revision : 0.1
T.R. Date : 2010.07.27

Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D Signature : X

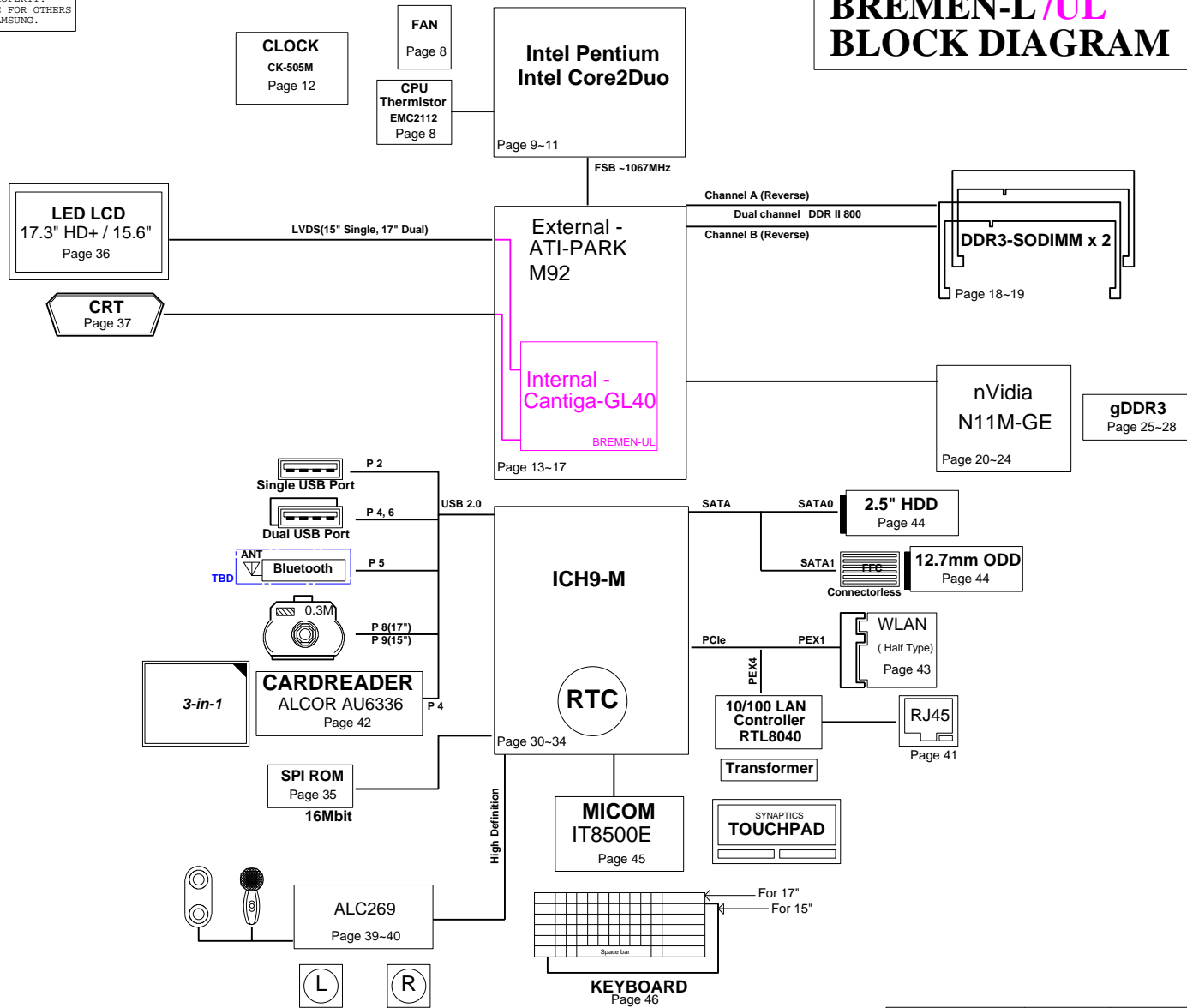
[Revision History]

1. The geom of APL5336 was changed because of shorted thermal pad.
2. The value of R881 & R841 was changed to 1ohm
3. The geom of BA61-01090A was changed because PEM fallied into hole.
4. Thermister was added at P5.0V of CRT port.
5. The property of Touchpad LED was changed.
6. 10kohm was pulled up on PCI3_STP#.
7. LAN Jack was changed to 3722-003036(DIP type).
8. Materials were moved to apply 'Concraft Memory Socket'.
Because Concraft memory socket is bigger than Foxconn.
9. VE ITEMS were applied.
10. APW7141 was changed to RT8209.
11. Diodes were addea at LAN signals.
12. P5.0V fill of ODD connector was changed for connectorless.
13. P5.0V_CRT source connected with USB Power S/W OUT2.

DRAW	Peng zhiyang	DATE	10/10/2008	Scala_15L MAIN COVER		SAMSUNG ELECTRONICS			
CHECK	Wu shijiang	DEV. STEP	ADV						
APPROVAL	BC Lee	REV	0.1						
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		PAGE	1	OF	59
						PART NO.		BA41-xxxxxA	

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BREMEN-L /UL BLOCK DIAGRAM



DRAW	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV			PART NO. BA41-xxxxxA
APPROVAL	BC Lee	REV	0.1			
MODULE CODE	undefined	LAST EDIT	July 14, 2010 20:53:00 PM	PAGE	2 OF 59	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	-
MICOM	Master		
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

USB PORT Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0	0	UHCL_3	6
UHCL_1	1	UHCL_4	7
UHCL_2	2	UHCL_5	8
UHCL_3	3		9
UHCL_4	4		10
UHCL_5	5		11

SATA Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-

PCI EXPRESS Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCIe1	WLAN	PCIe2	Wired LAN
PCIe3	-	PCIe4	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	14.318MHz	MICOM	CLOCK-Generator
Crystal	25MHz	LAN	

Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
VDC_ADPT	Primary DC system power supply (9 to 19V)	P1.05V_PEG -> P1.05V	P1.05V (Direct Media Interface Compensation)
VDC	Charger Reference Voltage Source	P5.0V	5.0V Power Rail (off in S3-S5)
VDC_CHG	3.3V supply for the RTC well.	P3.3V	3.3V Power Rail (off in S3-S5)
PRTC_BAT	5.0V always power well	P1.5V	1.5V Power Rail (off in S3-S5)
P5.0V_ALW	12.0V always power well	P1.05V	1.05V Power Rail (off in S3-S5)
P12.0V_ALW	Power Chip Reference	P0.75V	DDR3 Termination
P1.7V_VREF	Power Chip Reference	P5.0V_AUX	5.0V Power Rail (off in S4-S5)
P2.0V_VREF	Power Chip Reference	P3.3V_AUX	3.3V Power Rail (off in S4-S5)
P5.0V_VREF_FLT	Power Chip Reference	P1.5_AUX	1.5V Power Rail (off in S4-S5)
		CPU_CORE	Core Voltage for CPU
P3.3V_MICOM	Output voltage of RT8205AGQW (if VDC is removed, it will be off)	AUD_P5V	5.0V supply for Audio
LCD_VDD3V	3.3V (LED LCD)	P4.75V_AUD	Audio Analog Voltage
KBC3_CHG4.2V	To charge battery	P5.0V_STB	To charge USB device at sleep status
P1.2V_LAN	Internal Regulator's Power of LAN Controller	P5.0V_ODD	5.0V supply at SUB_ODD Board
P2.5V_LAN		EGFX_CORE	nVidia Graphic Chip power
P3.3V_MCD	3.3V (3-in-1 Socket)		

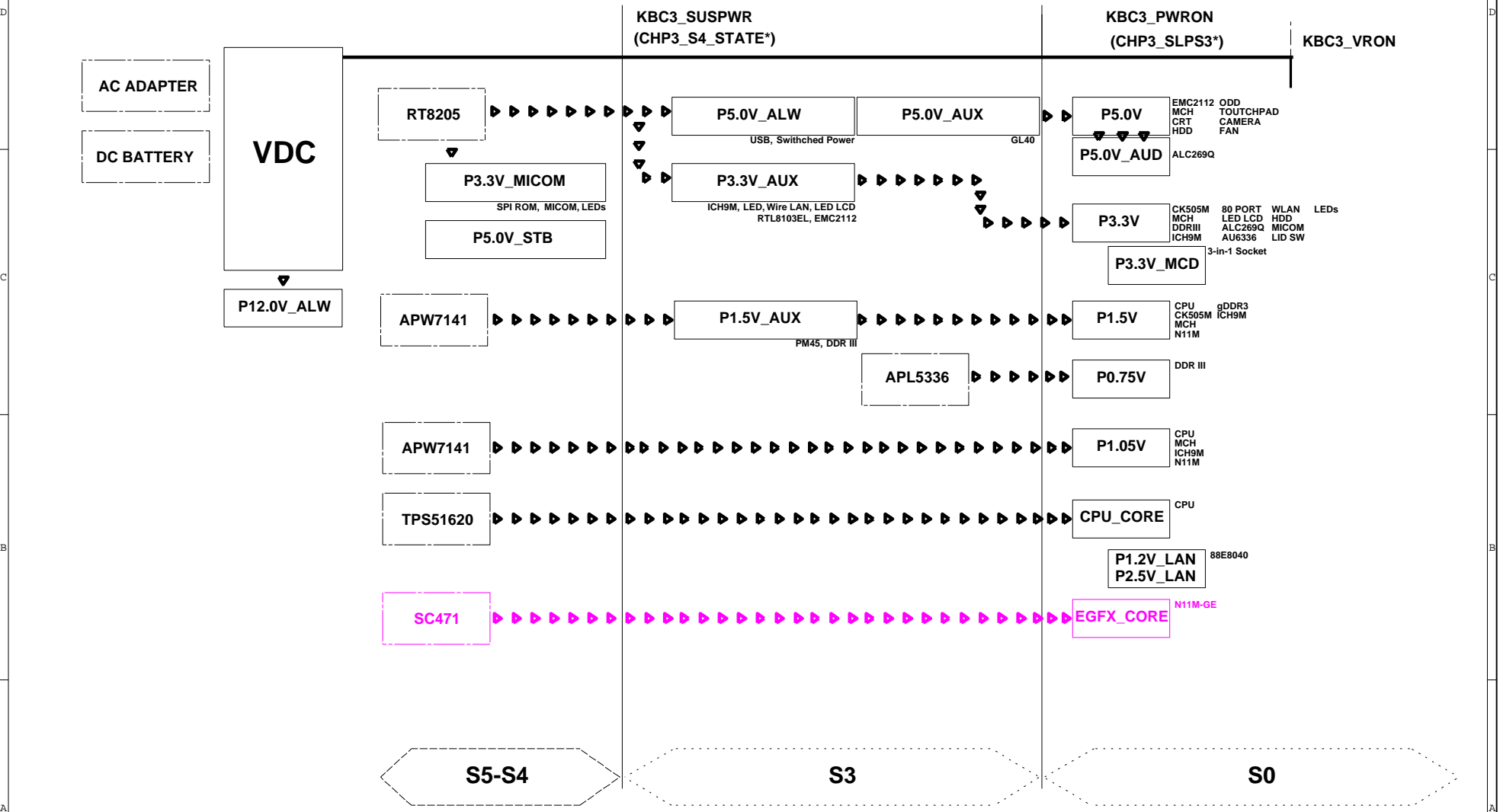
REVISION HISTORY

See rev notes for more information.

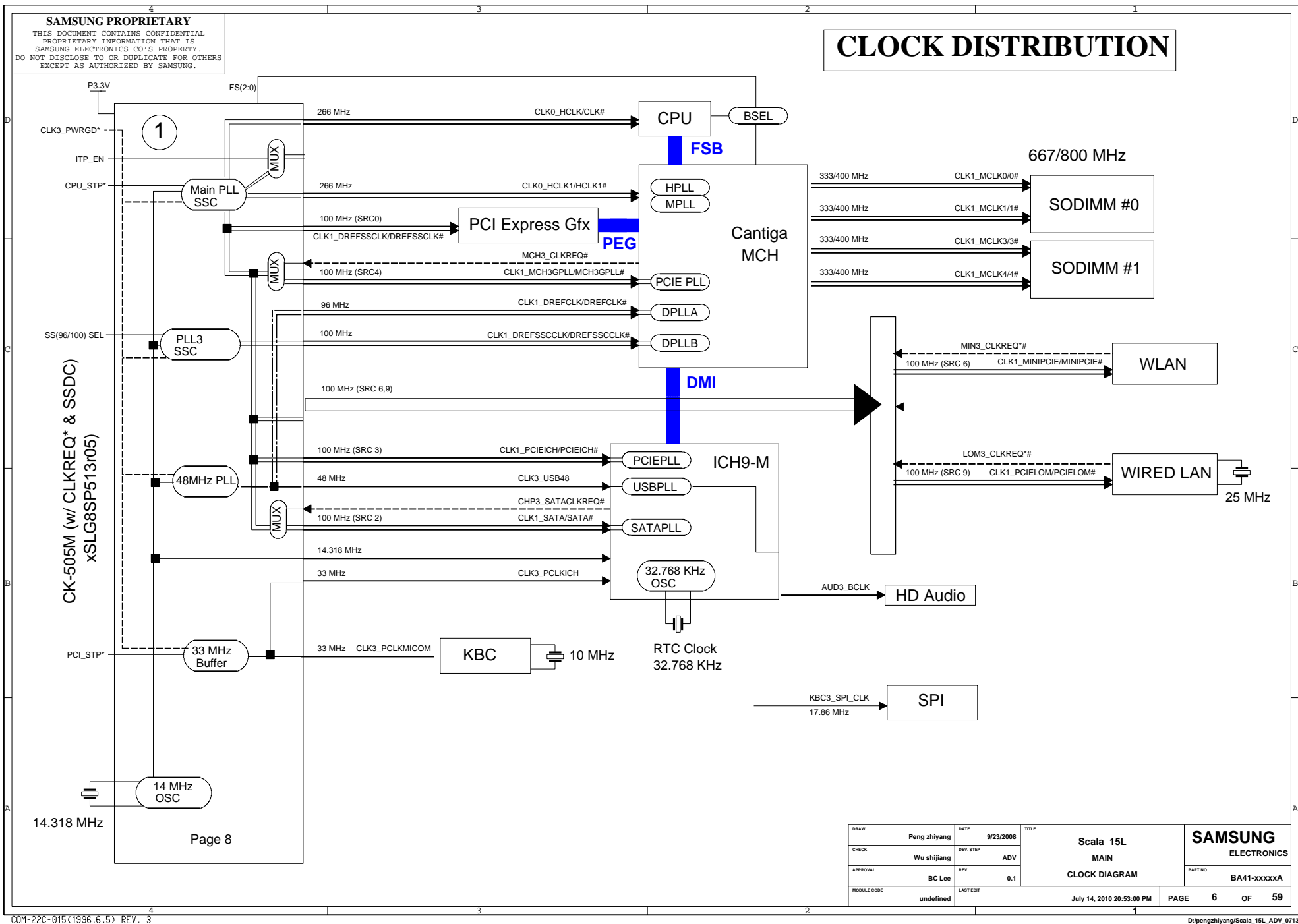
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CHECK	Wu shijiang	DEV. STEP	ADV						
APPROVAL	BC Lee	REV	0.1						
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		PAGE	3	OF	59
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POWER DIAGRAM

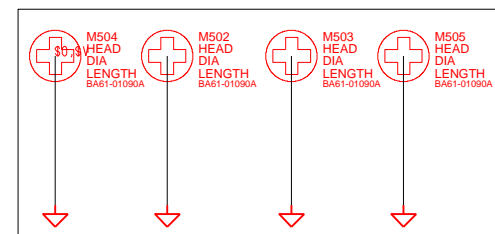
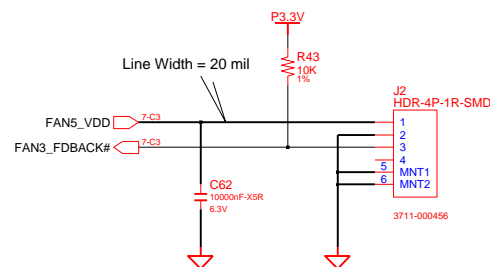


DRAW	Peng zhiyang	DATE	9/23/2008	Scala_15L MAIN POWER DIAGRAM		SAMSUNG ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	ADV				
APPROVAL	BC Lee	REV	0.1				
				PART NO.		BA41-XXXXXA	
MODULE CODE	undefined	LAST EDIT		July 14, 2010 20:53:00 PM		PAGE	4 OF 59



SHDN_SEL MODE	
0 HIGH Z	INTEL TR MODE AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

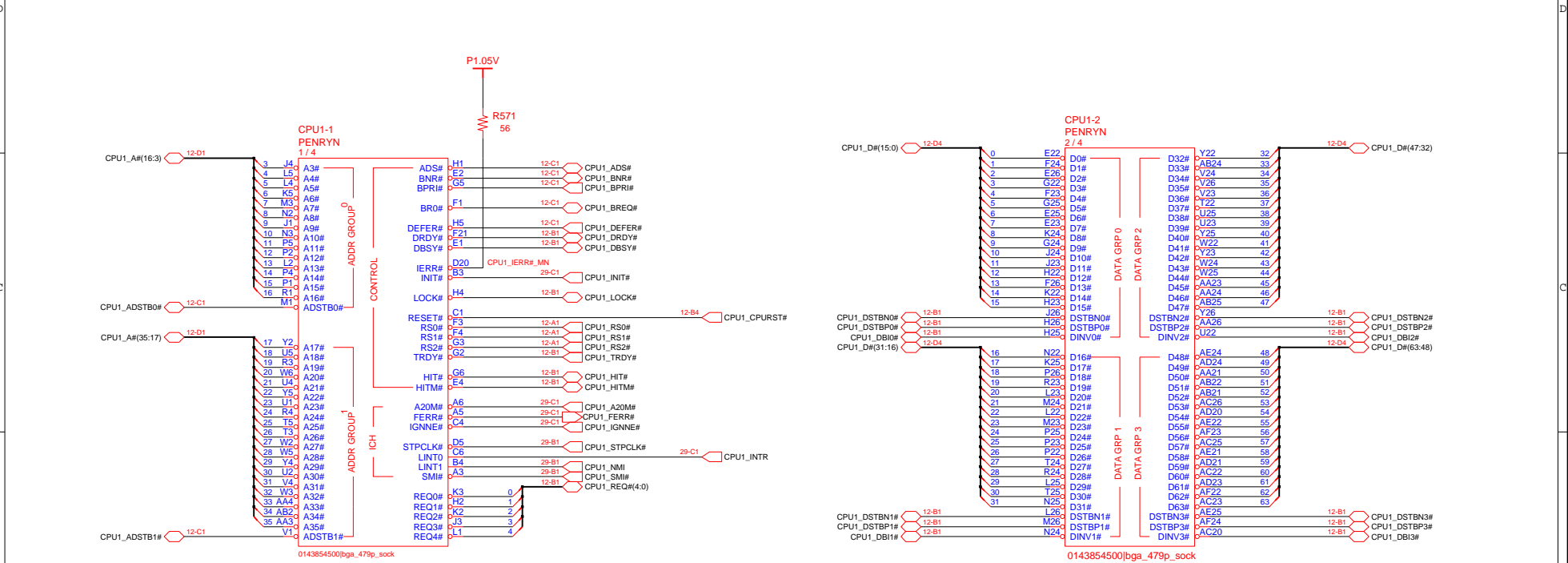
ADDRESSSEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb



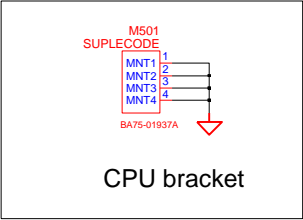
To support heatsink

DESIGN	Peng zhiyang	DATE	9/23/2008	TITLE Scala_15L THERMAL SENSOR THERMAL SENSOR EMC2112		SAMSUNG ELECTRONICS			
CHECK	Wu shijiang	DEV. STEP	ADV			PART NO. BA41-xxxxxxA			
APPROVAL	BC Lee	REV	0.1						
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		PAGE	7	OF	59

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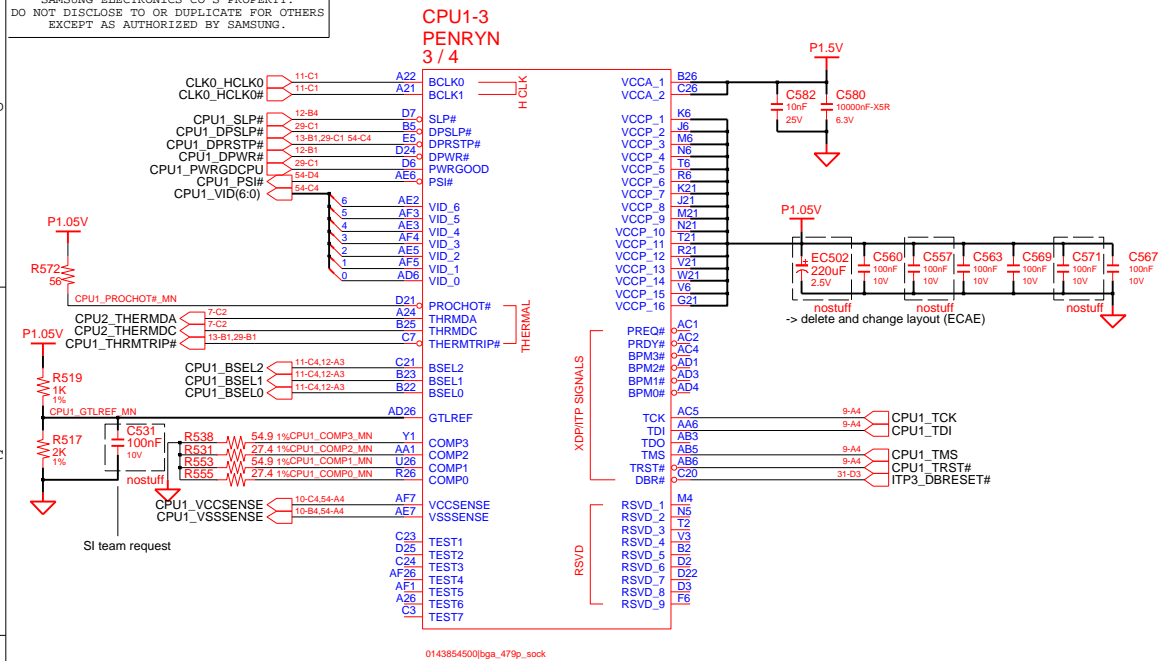


CPU Socket : 3704-001153

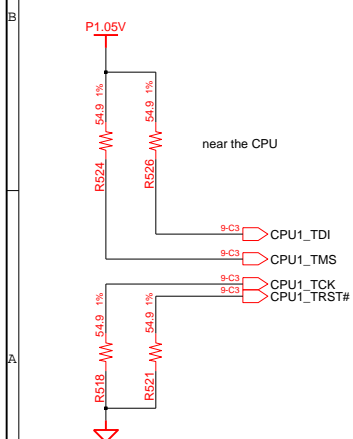


DRAW	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L
CHECK	Wu shijiang	DEV. STEP	ADV		CPU
APPROVAL	BC Lee	REV	0.1		PENRYN (1/3)
MODULE CODE	undefined	LAST EDIT	July 14, 2010 20:53:00 PM	PAGE	8 OF 59

SAMSUNG ELECTRONICS
PART NO. BA41-xxxxxA



FSC	FSB	FSA	FRQ
0	0	0	266M
0	1	0	200M
0	1	1	166M



BSEL

		Pull-down
FSB 1067 MHz FSB 800 MHz		BSEL0, BSEL1, BSEL2 BSEL0, BSEL2

CPU Core Voltage Table IMVP-6


Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 0	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 0 1	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 1 0 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 1 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 1 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 1 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 1 0 0 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 1 0 0 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 1 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with $Z_0=55\Omega$ trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with $Z_0=27.4\text{ohm}(55\text{ohm})$ trace shorter than $1/2"$ to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSense at the end of the line.
Route the VCC/VSSense as a $Z_0=55\text{ohm}$ traces with equal length.
Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away
(preferred 50mil) from any other signal. And GND via 100mil away
from each of the VCC/VSS test point vias.

DRAW	Peng zhiyang	DATE	9/23/2008	TITLE Scala_15L CPU PENRYN (2/3)	
CHECK	Wu shijiang	REV. STEP	ADV		
APPROVAL	BC Lee	REV	0.1		
MODULE CODE	undefined	LAST EDIT	July 14, 2010 20:53:00 PM		
				PART NO.	BA41-xxxxxA

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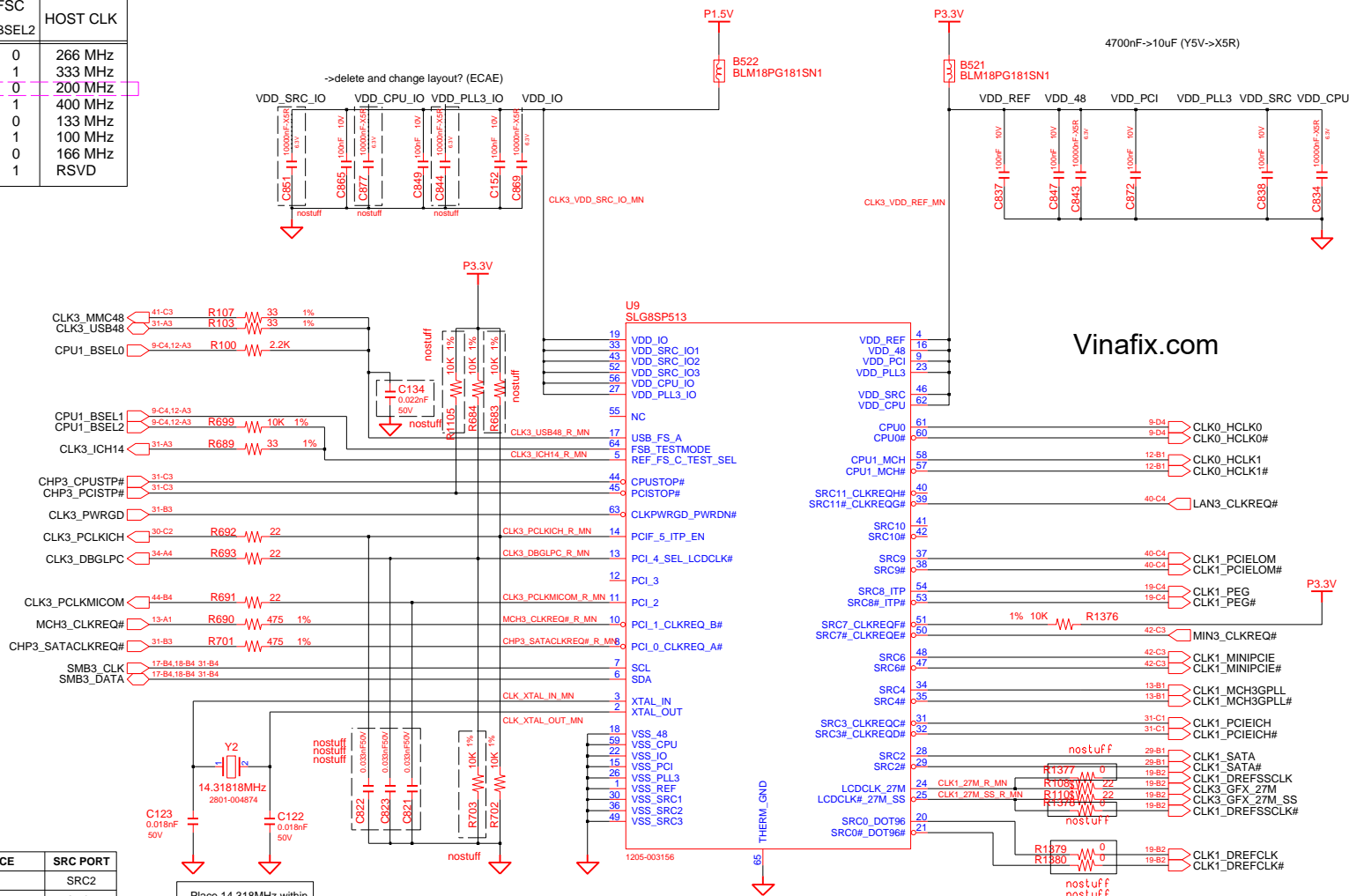
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CK505M

FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

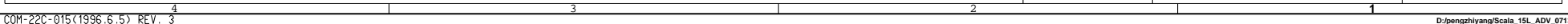


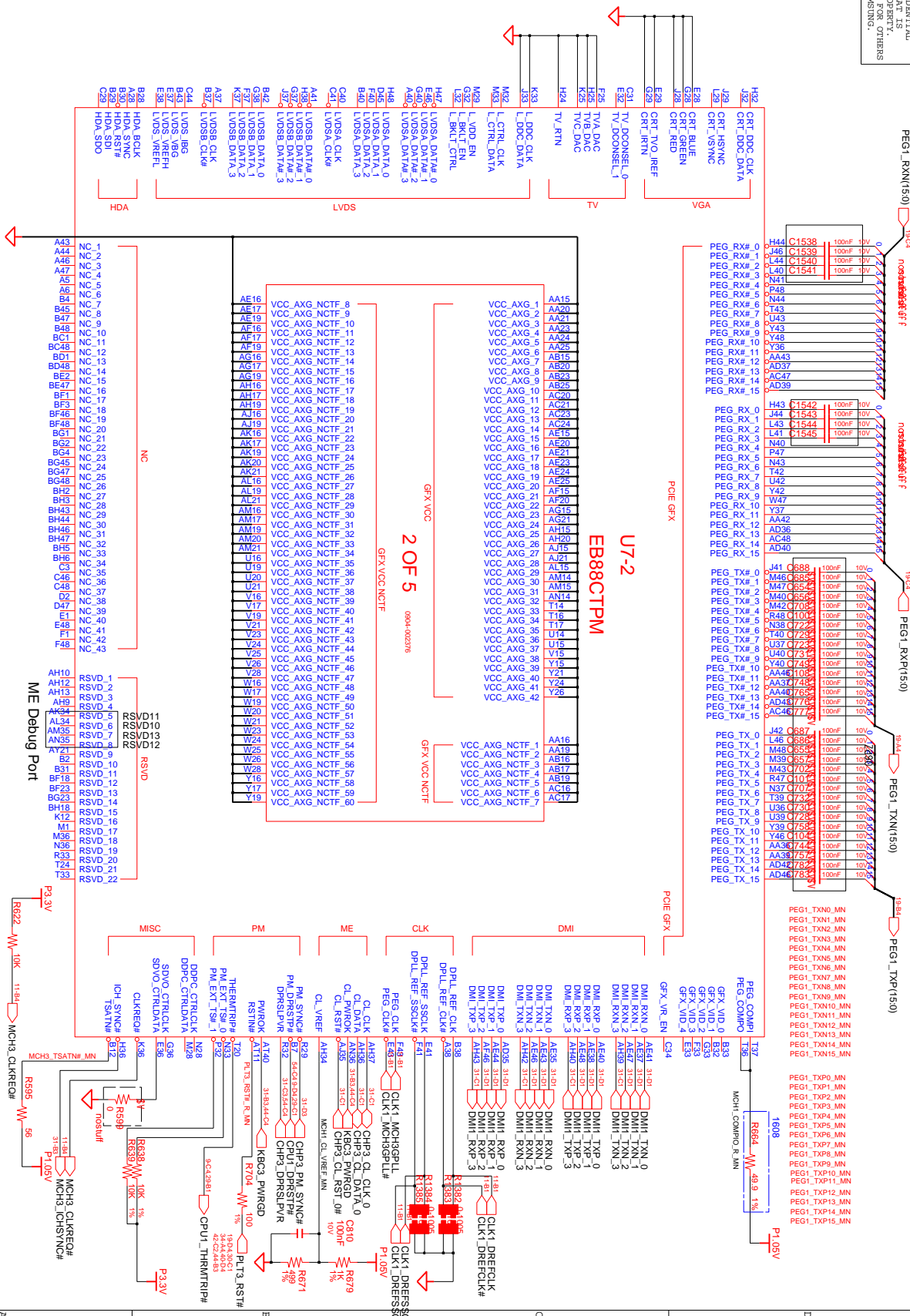
CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

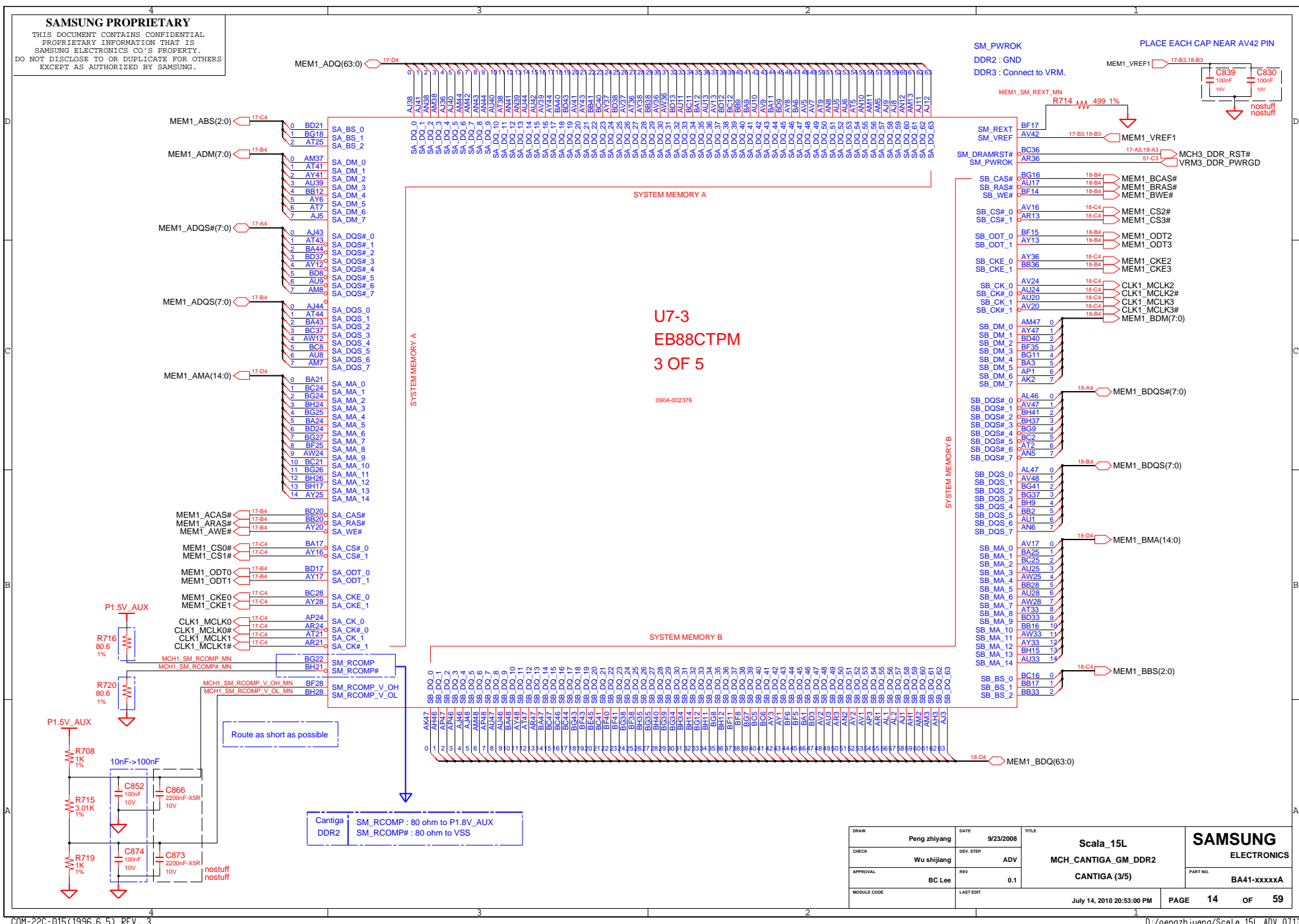
IDT : 1205-003159
SL : 1205-003533

DRAW	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L
CHECK	Wu shijiang	DEV. STEP	ADV	MAIN_CLOCK_CIRCUIT	SAMSUNG ELECTRONICS
APPROVAL	BC Lee	REV	0.1	CK_Clock_505M	PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	July 14, 2010 20:53:00 PM	PAGE	11 OF 59





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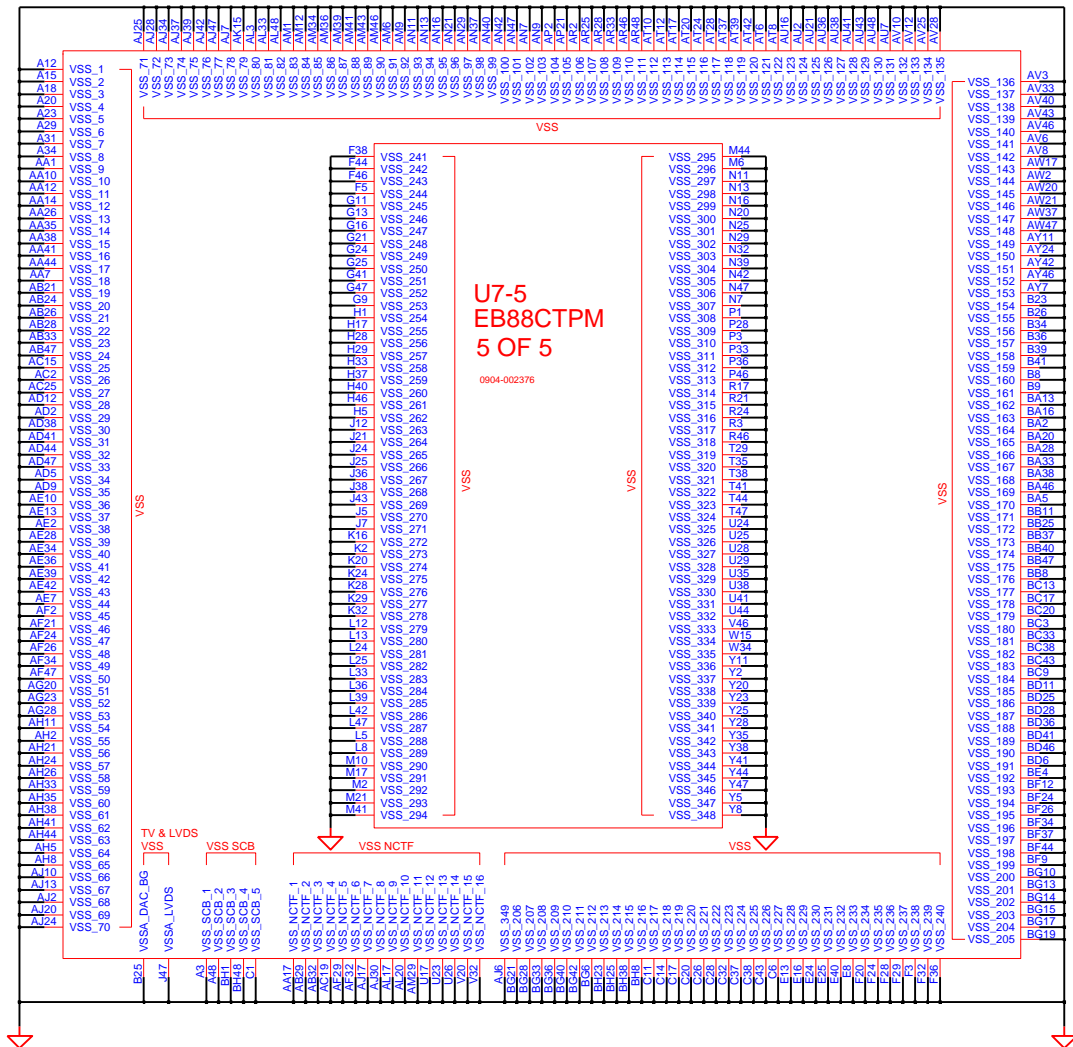


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DRAW	Peng zhiyang	DATE	9/23/2008	Scala_15L MCH_CANTIGA_GM_DDR2 CANTIGA (4/5)	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV		
APPROVAL	BC Lee	REV	0.1		
MODULE CODE			LAST EDIT		
				July 14, 2010 20:53:00 PM	BA41-xxxxxxA
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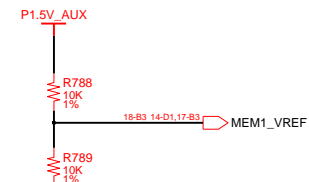
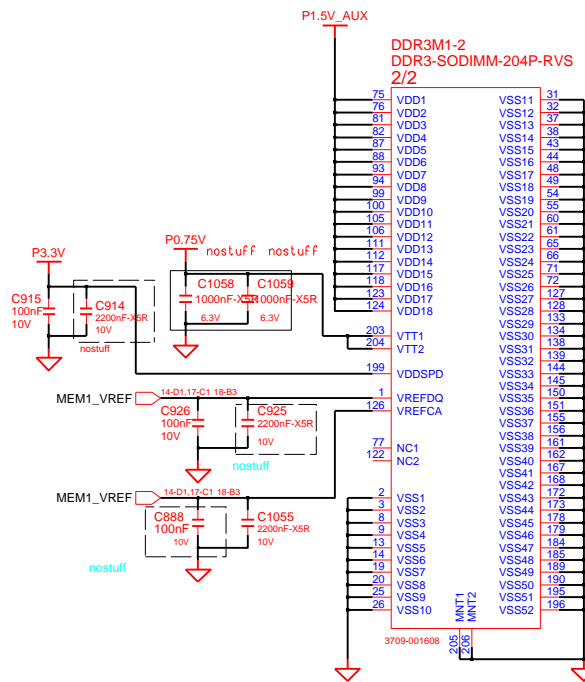
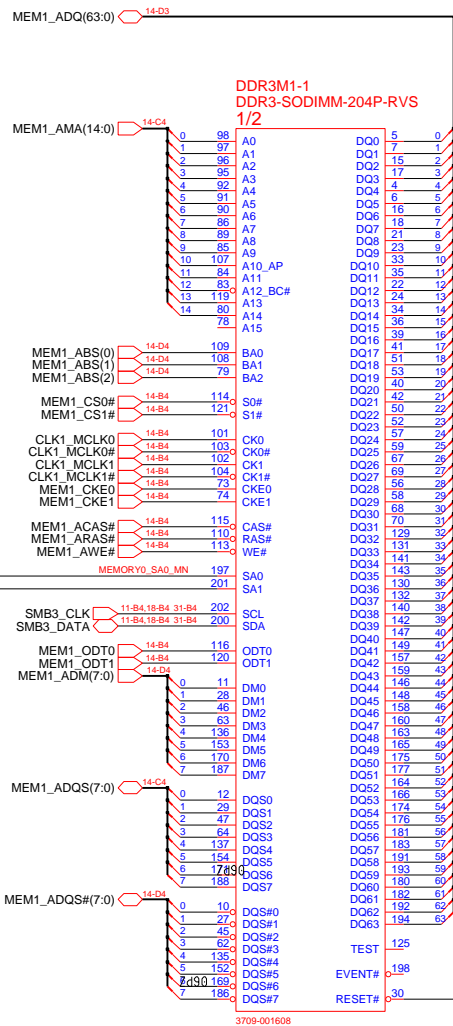
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DDR SO-DIMM #0

Height : 4 mm (REVERSED)

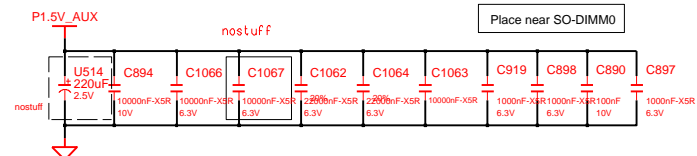
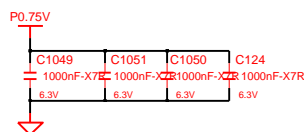
P/N : 3709-001533 (Molex)

P/N : 3709-001559 (Foxconn)



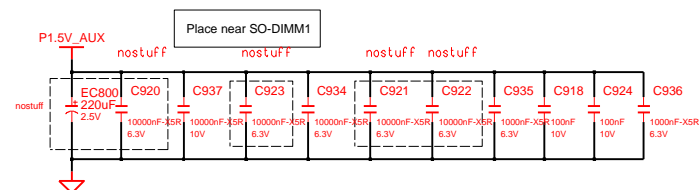
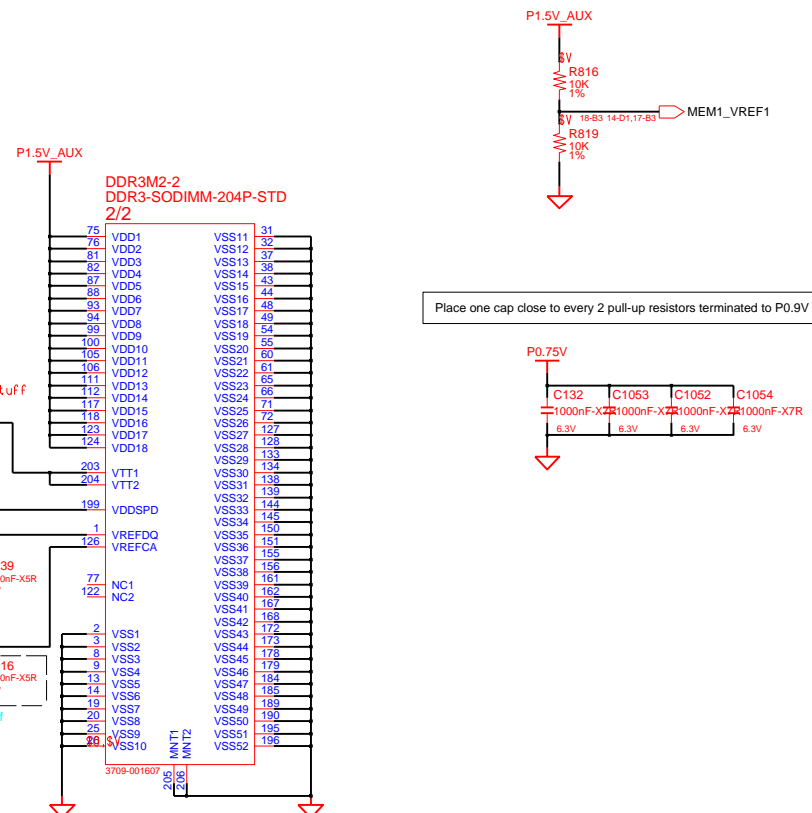
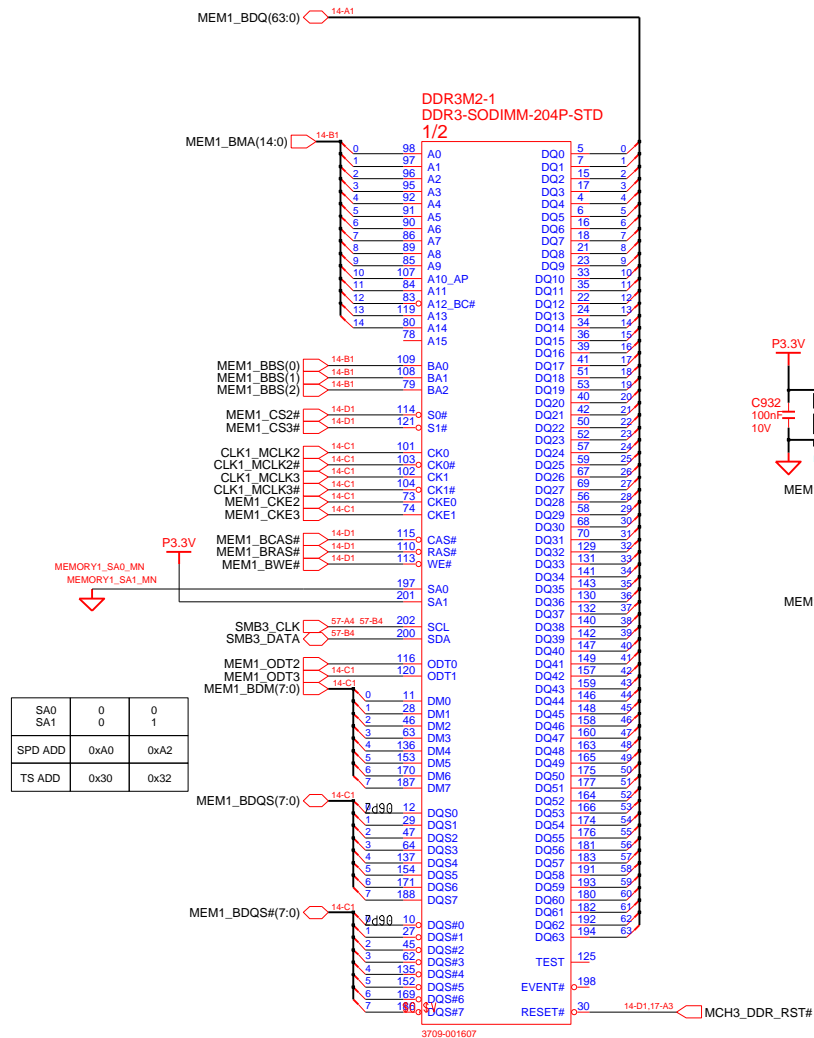
Place between two memory Connector

Place one cap close to every 2 pull-up resistors terminated to P0.9V



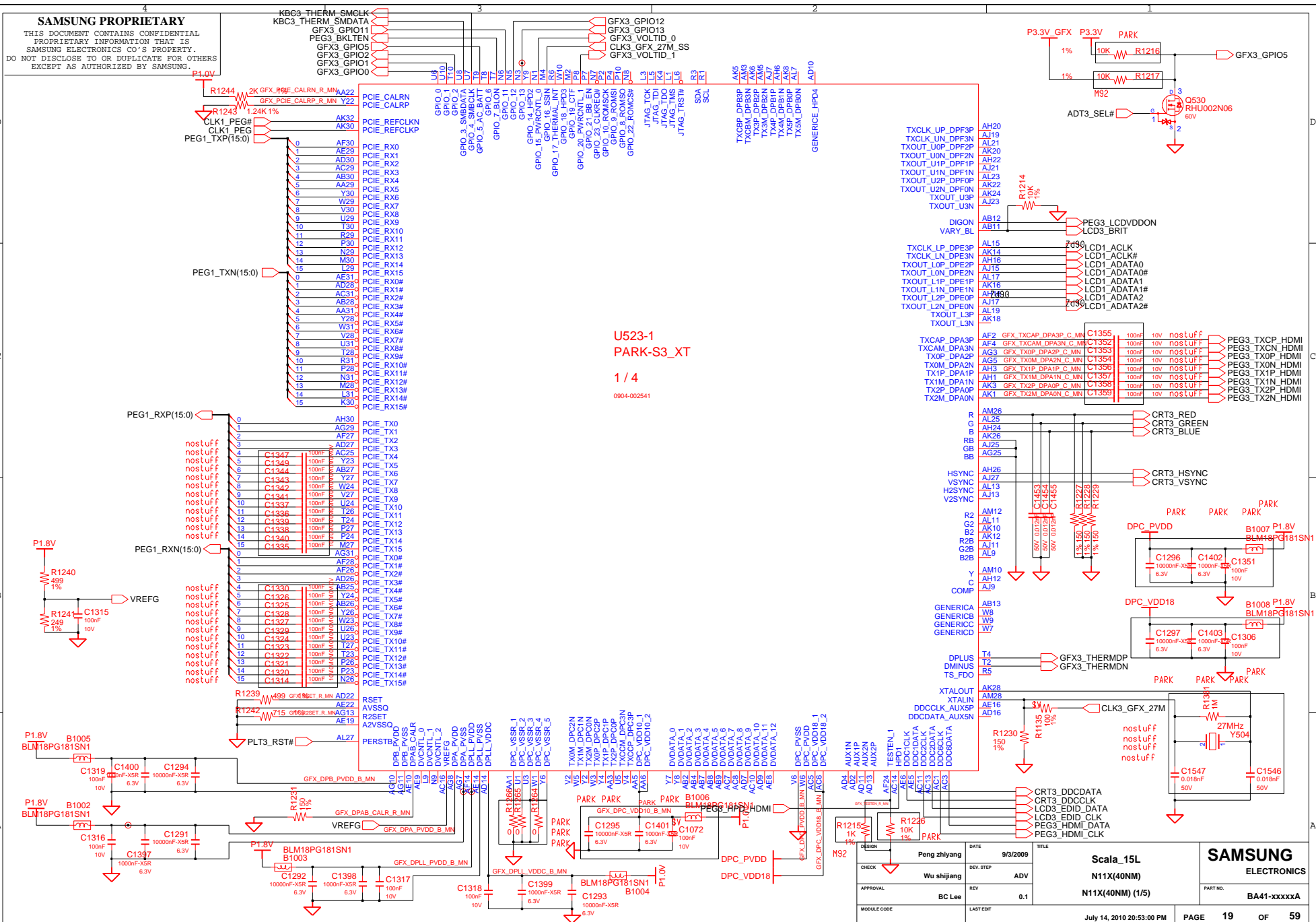
DRAW	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	Wu shijiang	DEV. STEP	ADV		SODIMM_DDR2	
APPROVAL	BC Lee	REV	0.1		SODIMM_DDR2 #1	
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		
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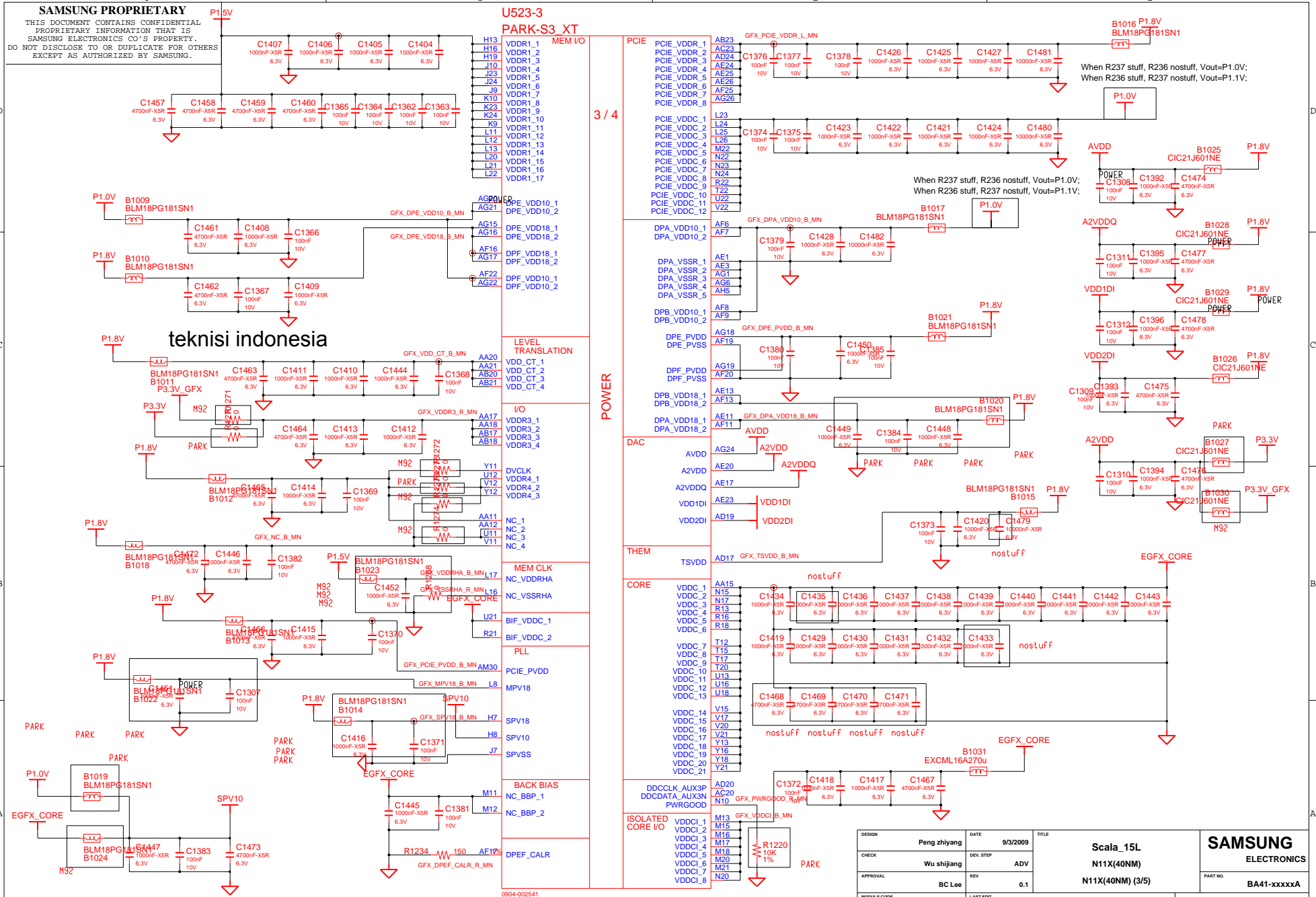
Height : 4 mm (STANDARD)
P/N : 3709-001532 (Molex)
P/N : 3709-001560 (Foxconn)



DRAW	Peng zhiyang	DATE	9/23/2008	Scala_15L SODIMM_DDR2 SODIMM_DDR2 #2	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV		
APPROVAL	BC Lee	REV	0.1		
MODULE CODE			LAST EDIT		
				July 14, 2010 20:53:00 PM	BA41-xxxxxA
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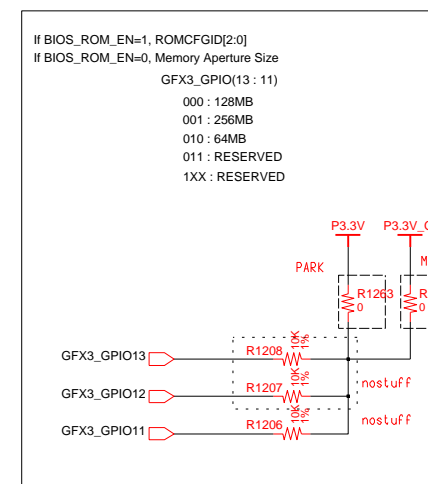
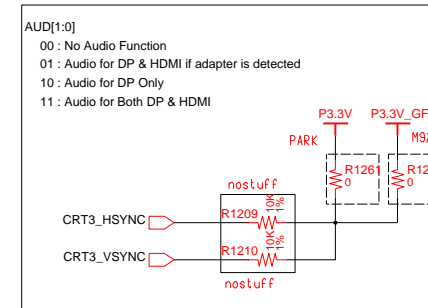
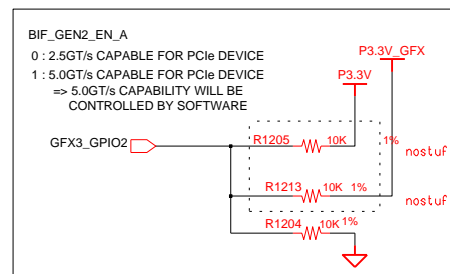
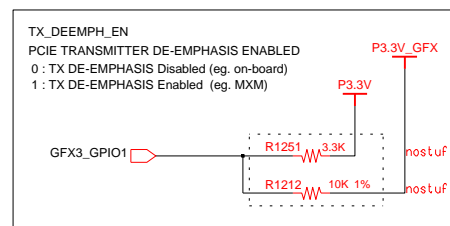
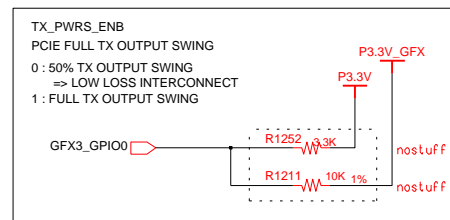
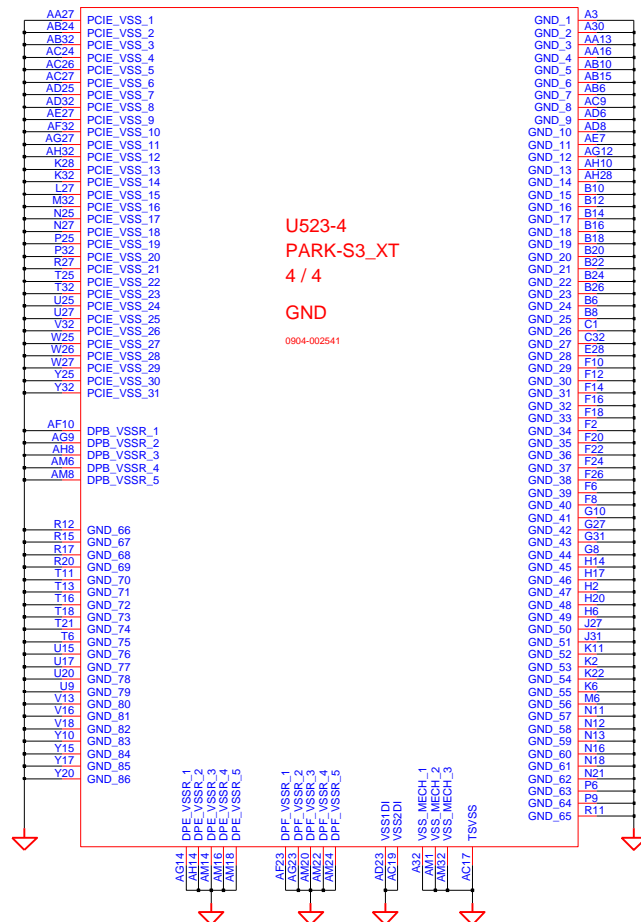




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PARK & M92 Straps

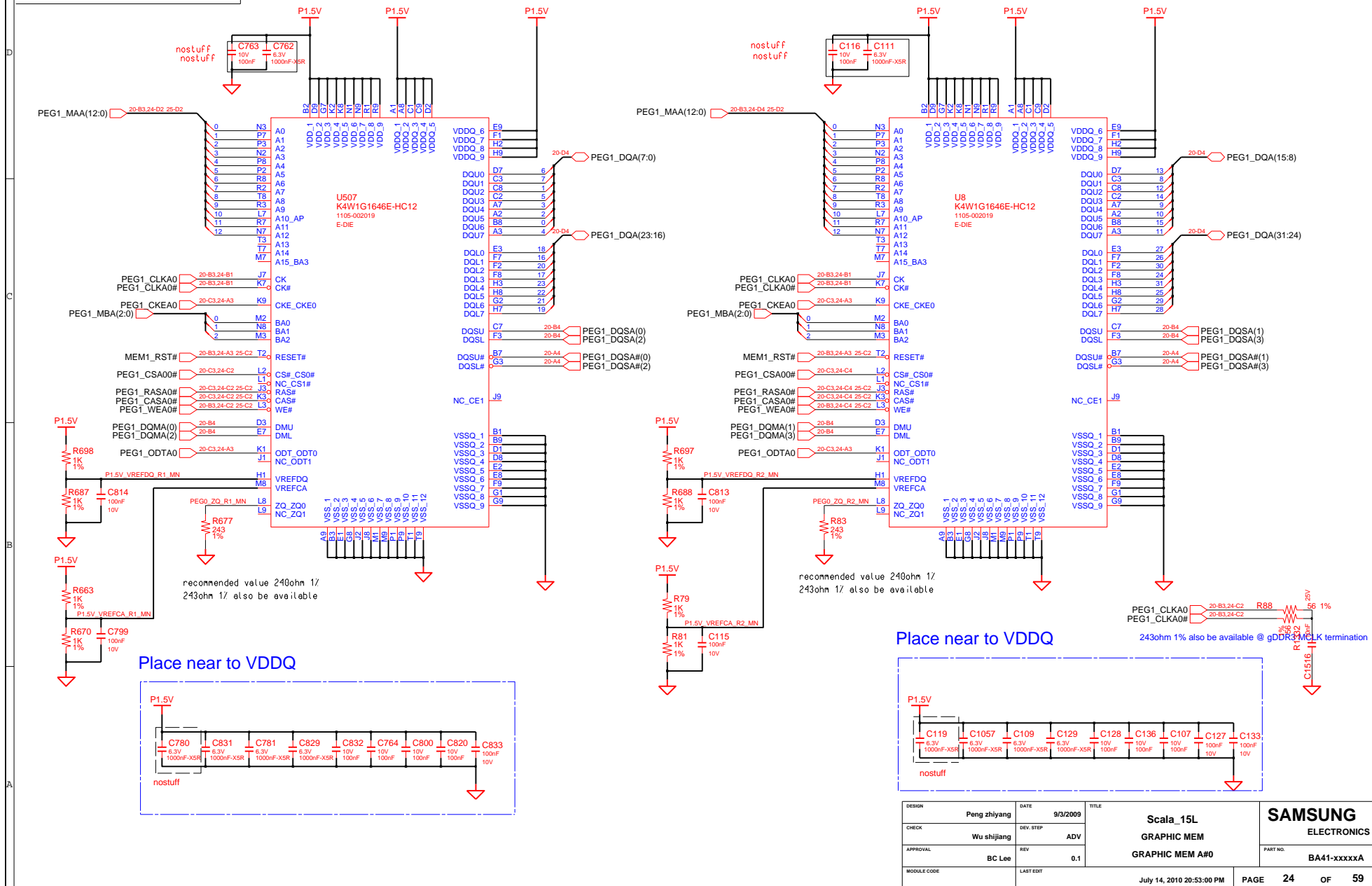


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APPROVAL	BC Lee	REV	0.1		N11X(40NM) (4/5)	
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM	PAGE 22 OF 59	

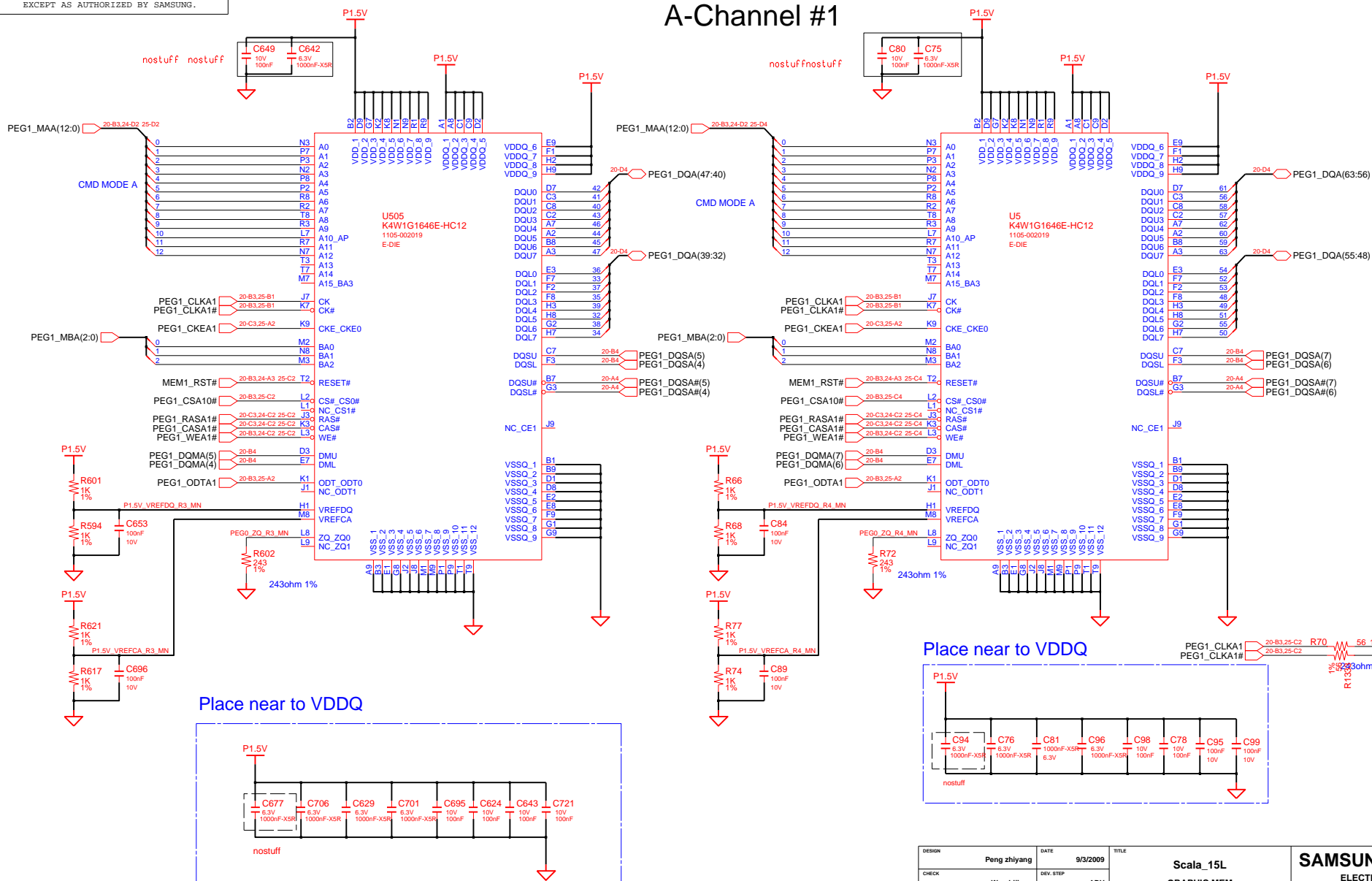
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DESIGN	Peng zhiyang	DATE	9/3/2009	TITLE		Scala_15L N11X(40NM) N11X(40NM) (5/5)		SAMSUNG ELECTRONICS																																			
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APPROVAL	BC Lee	REV	0.1																																								
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		PAGE 23		OF 59																																			
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A-Channel #0



A-Channel #1



DESIGN	Peng zhiyang	DATE	9/3/2009	TITLE Scala_15L GRAPHIC MEM GRAPHIC MEM A#1	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV		
APPROVAL	BC Lee	REV	0.1		
MODULE CODE	LAST EDIT				
				July 14, 2010 20:53:00 PM	PAGE 25 OF 59

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<div> <div>D</div> <div>C</div> <div>B</div> <div>A</div> </div>																																	
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CHECK	Wu shijiang	DEV. STEP	ADV																														
APPROVAL	BC Lee	REV	0.1			PART NO. BA41-xxxxxA																											
MODULE CODE	LAST EDIT					July 14, 2010 20:53:00 PM																											
						PAGE 26 OF 59																											

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1

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D

C

B

A

DESIGN	Peng zhiyang	DATE	9/3/2009	TITLE	Scala_15L GRAPHIC MEM GRAPHIC MEM C#1	SAMSUNG ELECTRONICS
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APPROVAL	BC Lee	REV	0.1			PART NO.
MODULE CODE				LAST EDIT	July 14, 2010 20:53:00 PM	PAGE 27 OF 59

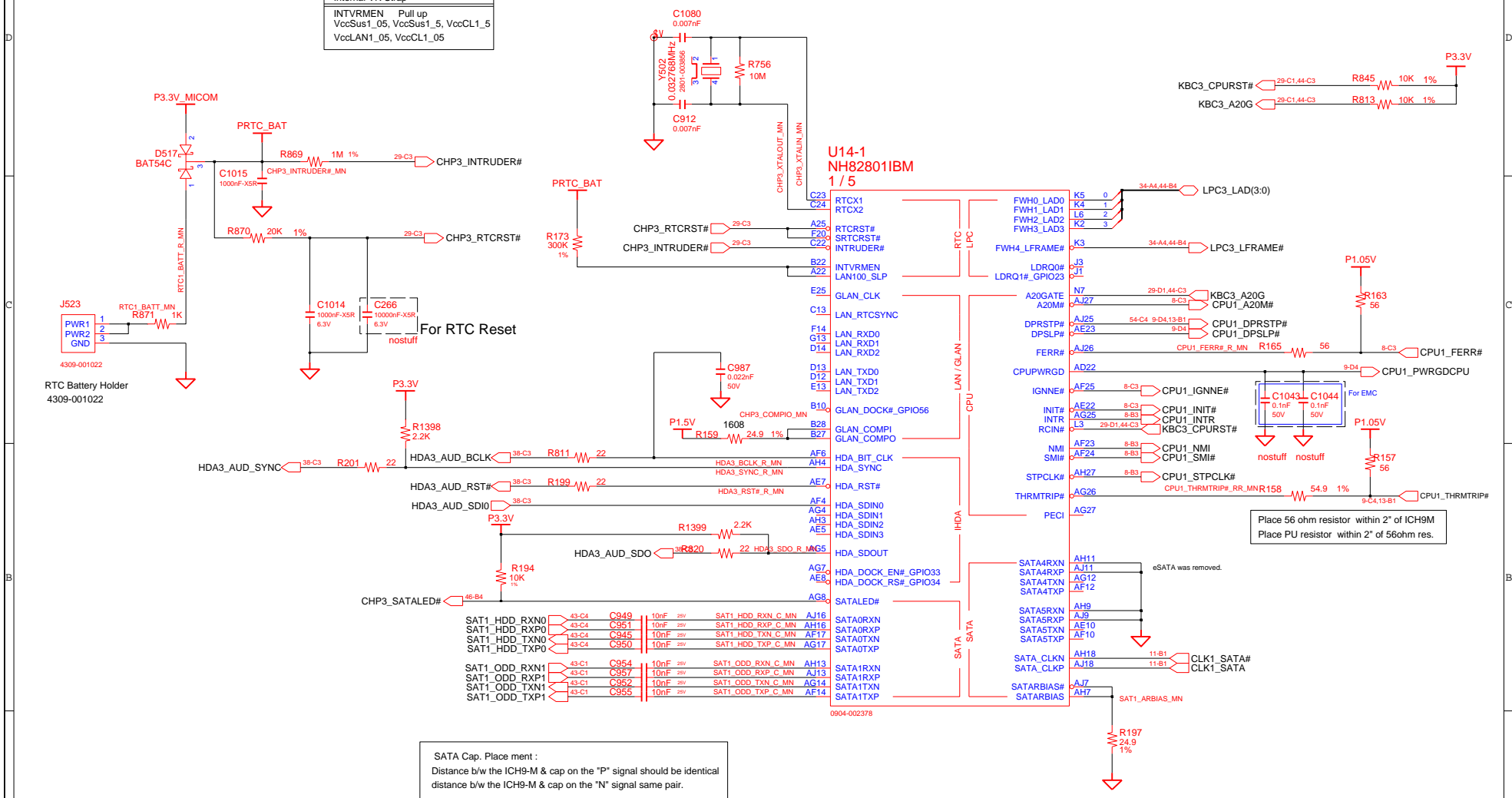
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DESIGN	Peng zhiyang	DATE	9/3/2009	TITLE	Scala_15L	<div>SAMSUNG</div> ELECTRONICS		
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APPROVAL	BC Lee	REV	0.1					
MODULE CODE	LAST EDIT					July 14, 2010 20:53:00 PM	PAGE	28

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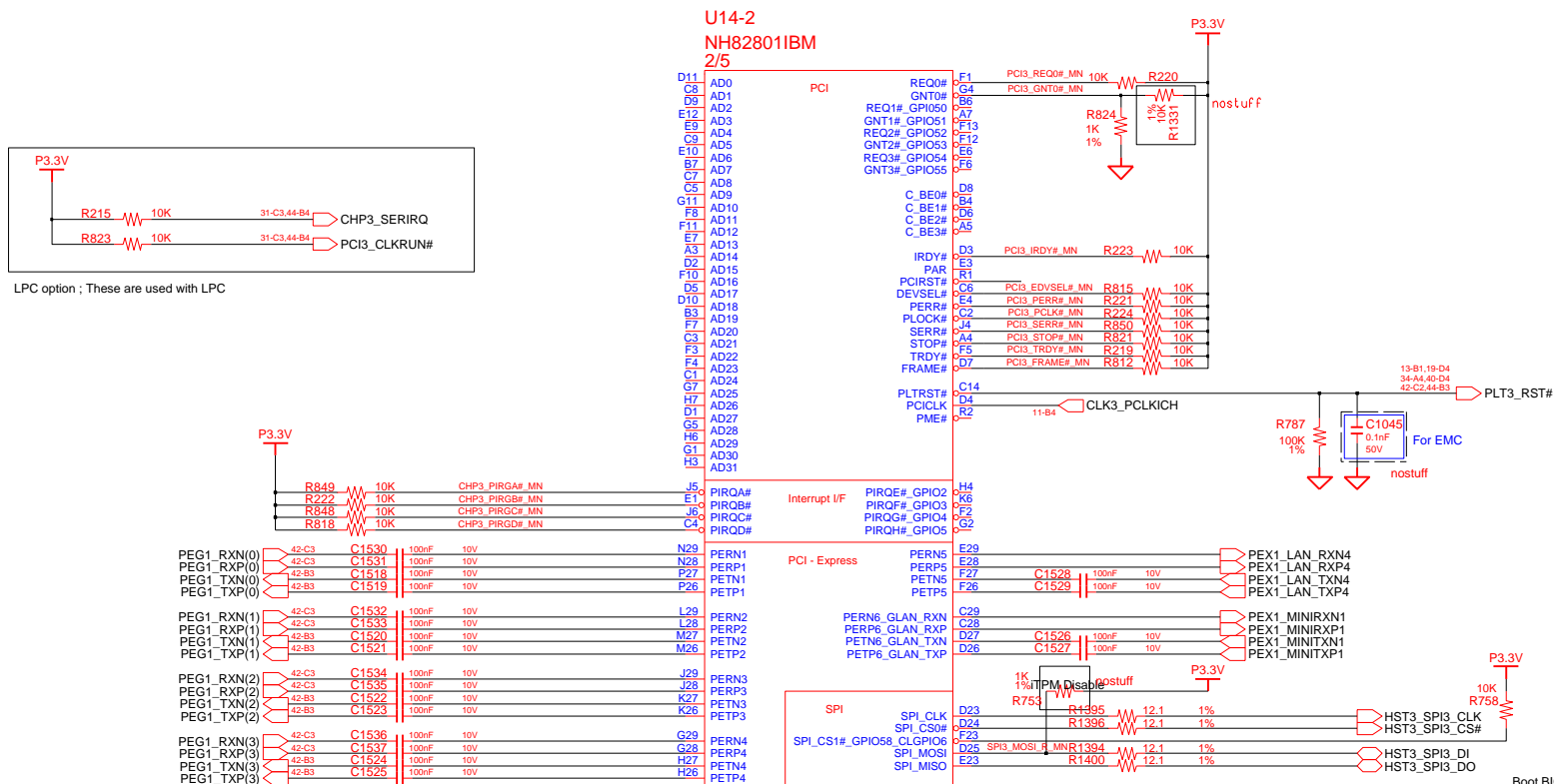
Internal VR Strap
INTVRMEN Pull up VccSus1_05, VccSus1_5, VccCL1_5 VccLAN1_05, VccCL1_05



DRAW	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L ICH_9M_B ICH9-M (1/5)	
CHECK	Wu shijiang	REV. STEP	ADV			
APPROVAL	BC Lee	REV	0.1			
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		PART NO. BA41-xxxxxA
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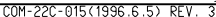
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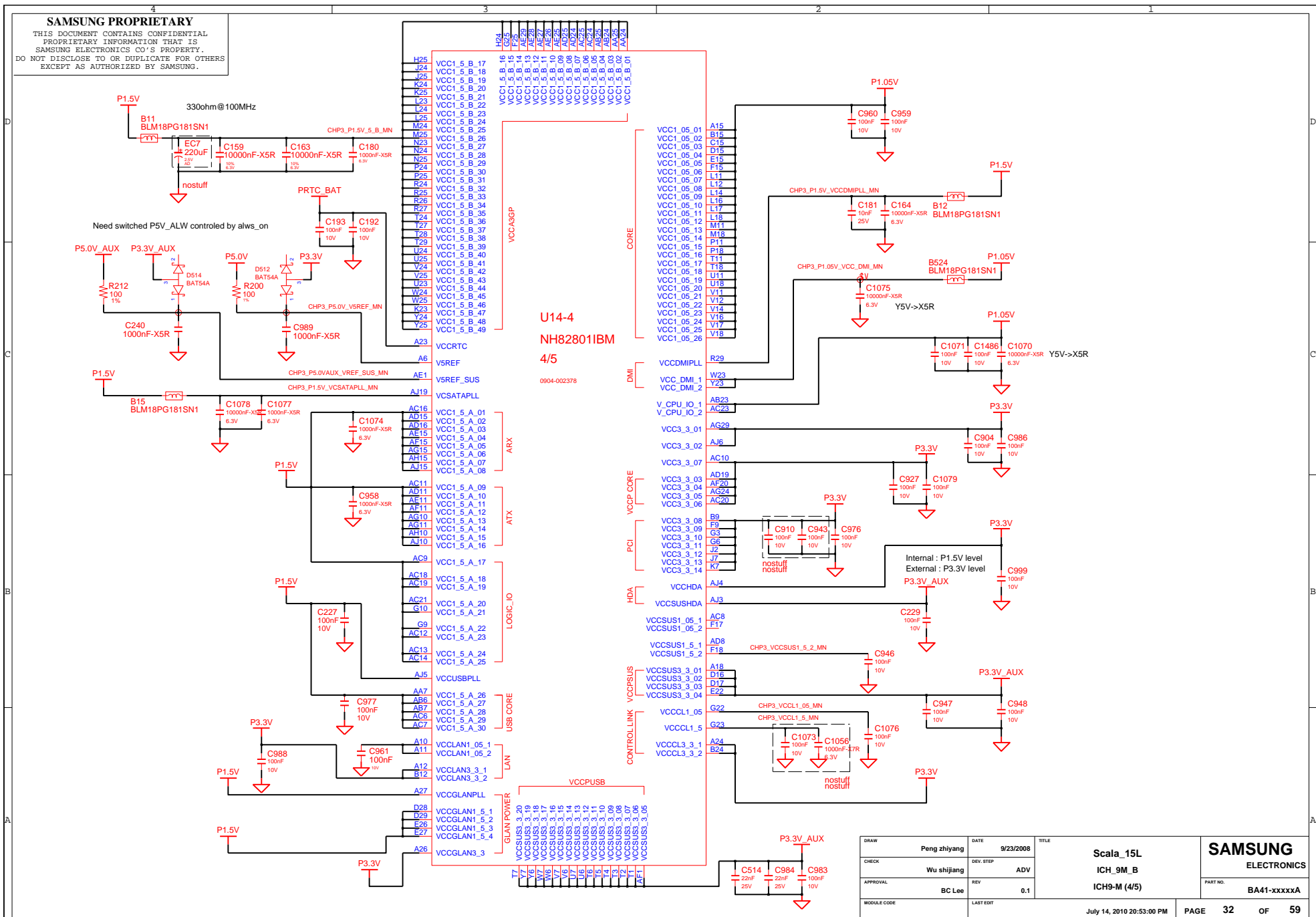


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APPROVAL	BC Lee	REV	0.1		ICH9-M (2/5)	
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PAGE 30 OF 59						PART NO. BA41-xxxxxA

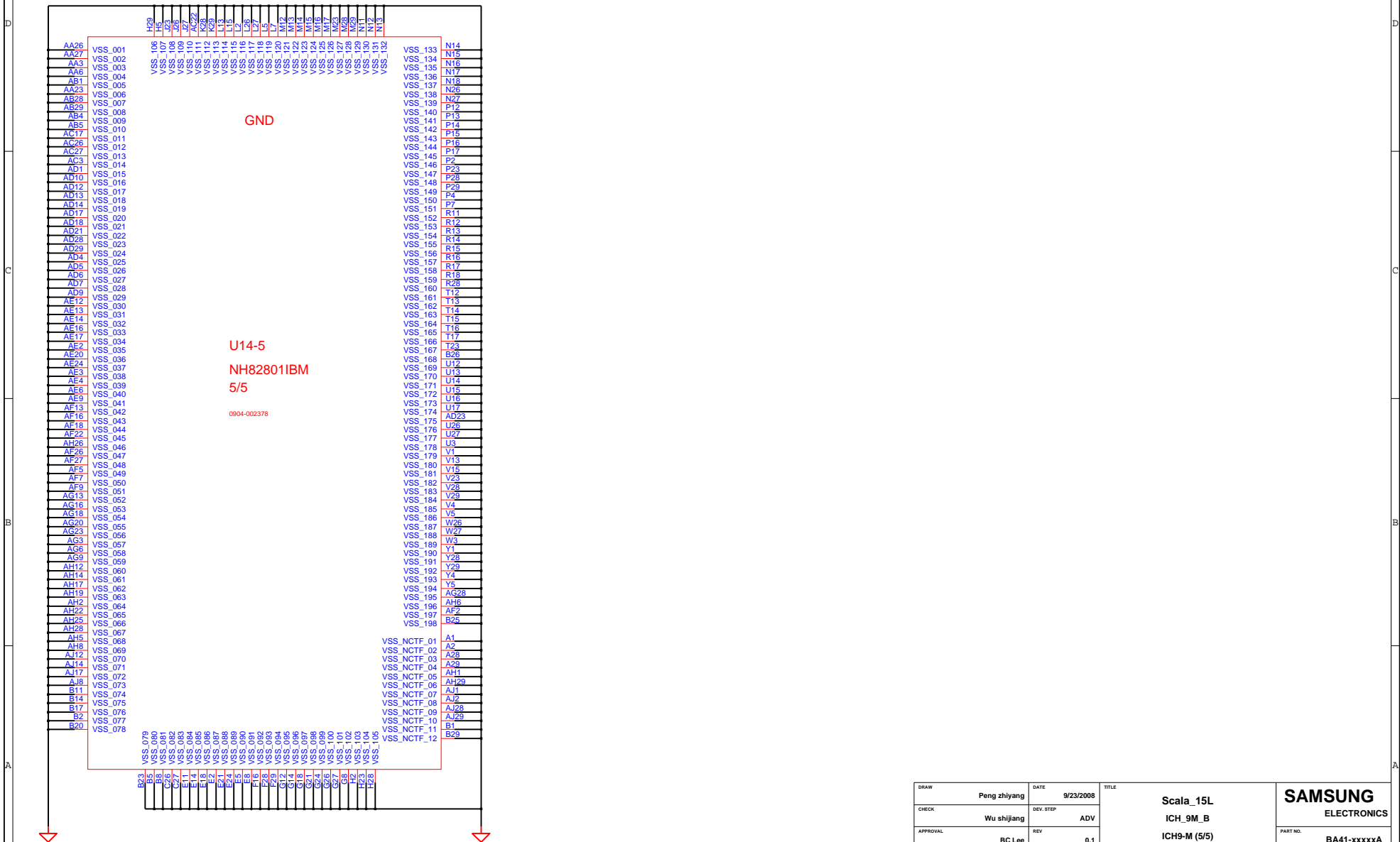
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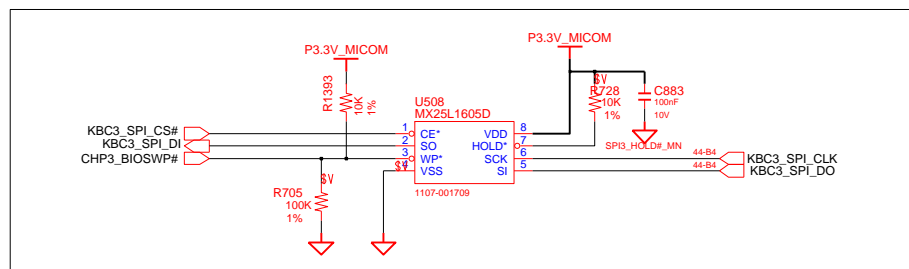


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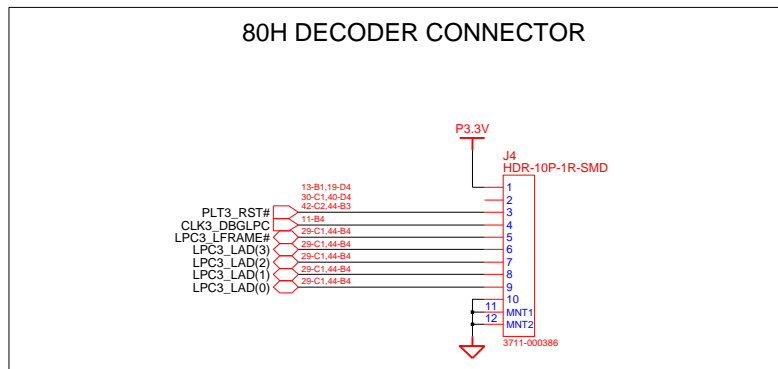
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SPI_BIOS_ROM

16MBit



80H DECODER CONNECTOR

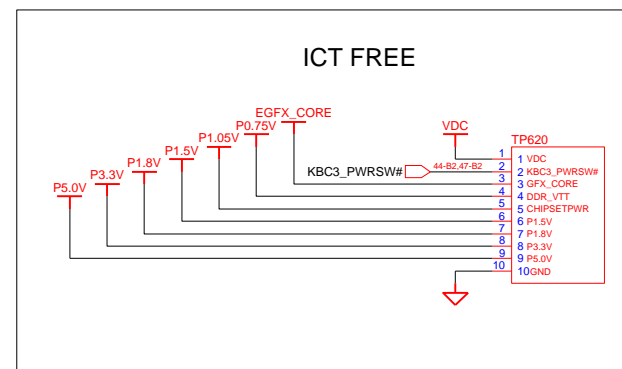


```
02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT SYSTEM HW
08 INIT CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU REG
0B CPU CACHE ON
0C INIT CACHE TO POST
0E INIT I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT. POWER MANAGER
11 LOAD ALTERNATE REG
13 PCI BUS MASTER RESET

14 WITH INITIAL POST VALUE
16 INIT. KEYBOARD CONTROLLER
18 CHECK CHECKSUM
19 8254 TIMER INIT
1A 8237 DMA CONTROLLER INIT.
1C RESET INTERRUPT CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TEST CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTERNATE REG. WITH CMOS VALUE
42 INIT. INTERRUPT VECTOR
44 INIT. BIOS INTERRUPT
46 CHECK ROM COPYRIGHT NOTICE
47 INIT. I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT. PCI BUS AND DEVICE
4A INIT. ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
59 DISPLAY PRESS SETUP
5C TEST RAM BETWEEN 812K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1

66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD ERROR
78 SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSOR IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT RS232C
84 DETECT AND INSTALL EXT PARALLEL
86 RE-INIT. ON-BOARD I/O PORT
88 INIT. BIOS DATA ROM
8A INIT. EXTENDED BIOS DATA AREA
8C INIT. FDD CONTROLLER
8E SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT. TYPEMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DIMM INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
C2 INTERRUPT HANDLER ERROR
C4 UNKNOWN INTERRUPT ERROR
C6 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
D9 ENABLE NMI
E0 INIT. HDD CONTROLLER
E1 INIT. LOCAL BUS HDD CONTROLLER
E2 JUMP TO USER PATCH 2
E4 DISABLE A20 ADDRESS LINE
E6 CLEAR HUGE ES SEGMENT REG.
E8 SEARCH FOR OPTION ROMS
```

ICT FREE



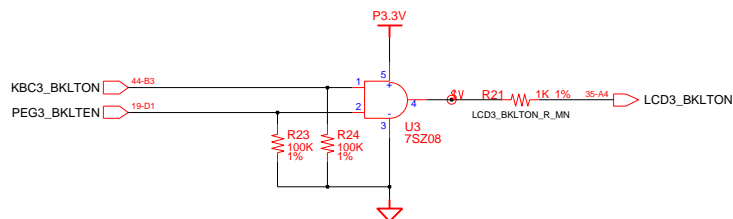
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APPROVAL	BC Lee	REV	0.1		SPI_BIOS_ROM	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxA
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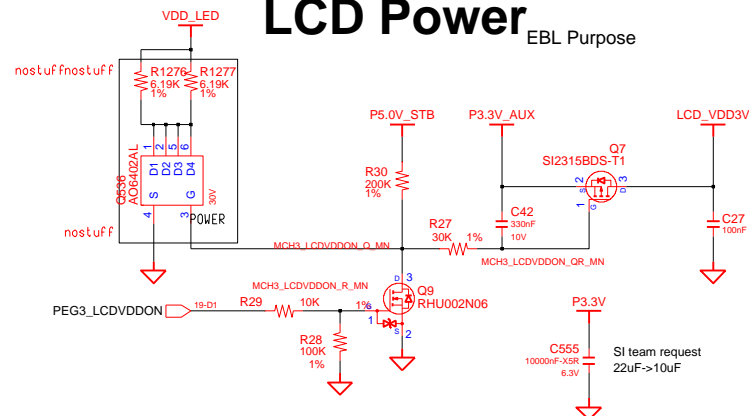
LVDS

Backlight On

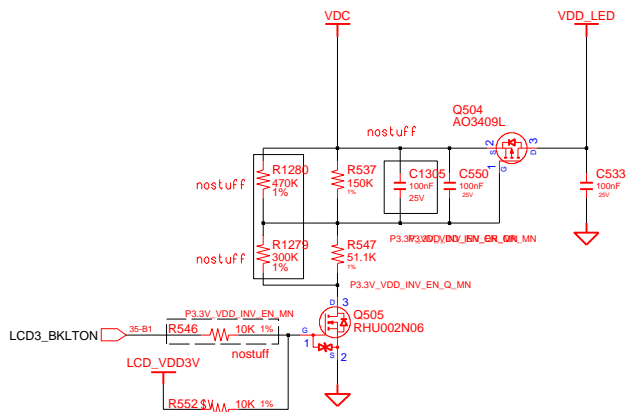


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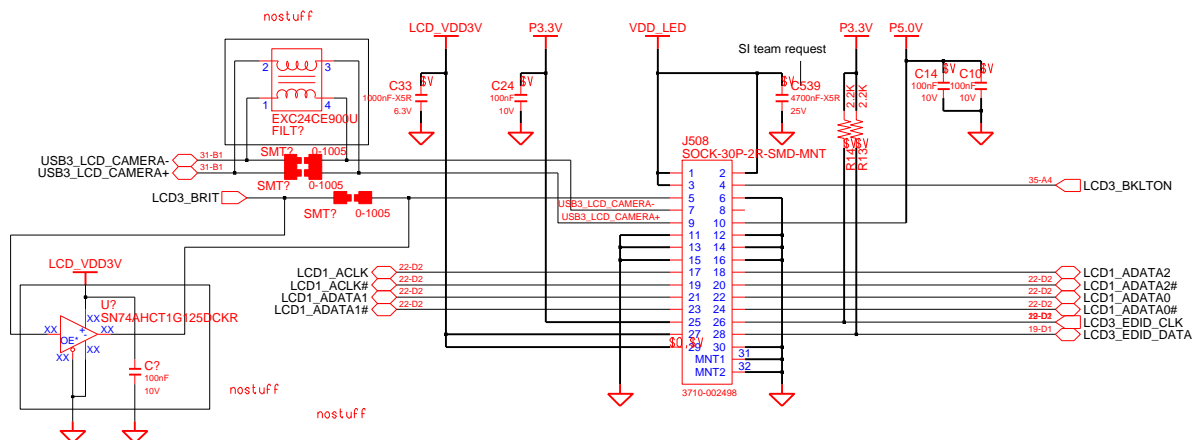
EBL Purpose



LED Power



LCD Connector



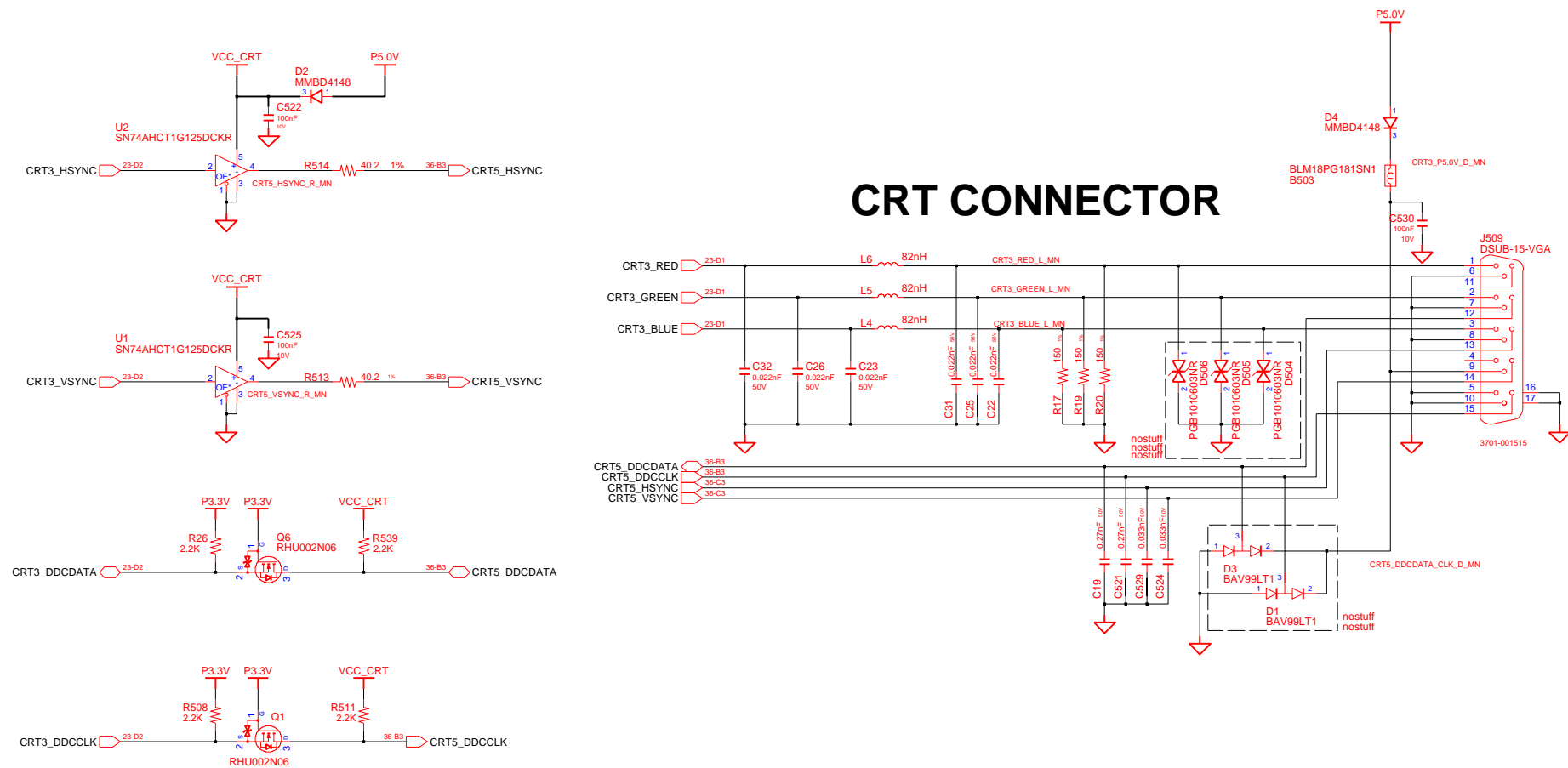
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APPROVAL	BC Lee	REV	0.1		LVDS	
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		
PAGE 35 OF 59						

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CRT

CRT CONNECTOR



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

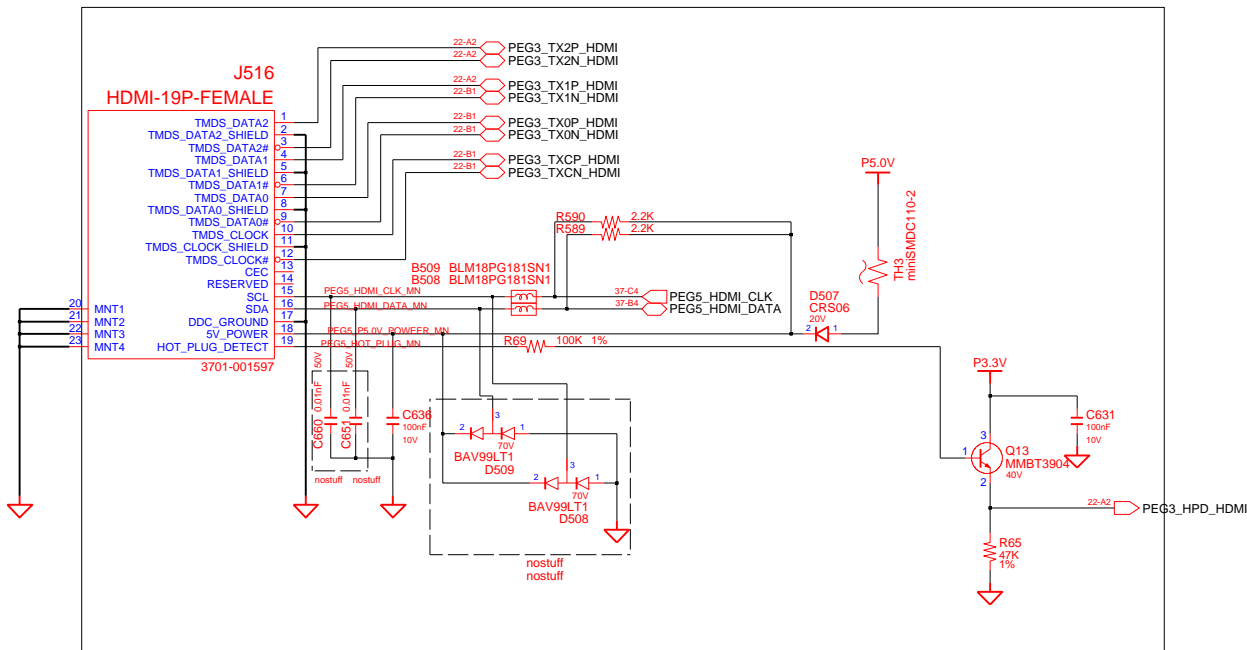
Vinafix.com

DESIGN	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	Wu shijiang	DEV. STEP	ADV		GRAPHICS_IF	
APPROVAL	BC Lee	REV	0.1		CRT	
MODULE CODE		LAST EDIT				
July 14, 2010 20:53:00 PM						PAGE 36 OF 59

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nostuff	nostuff	nostuff	nostuff	nostuff	nostuff
nostuff	nostuff	nostuff	nostuff	nostuff	nostuff

The schematic diagram illustrates the HDMI input circuit. It features a differential signal path from PEG3_HDMI_DATA (pin 24-B2) and PEG5_HDMI_DATA (pin 37-C2) through a resistor network (R635, 2.2K) and a buffer (Q509, RHU002N06) to the HDMI input pins (19, 20). Power is supplied by P3.3V.

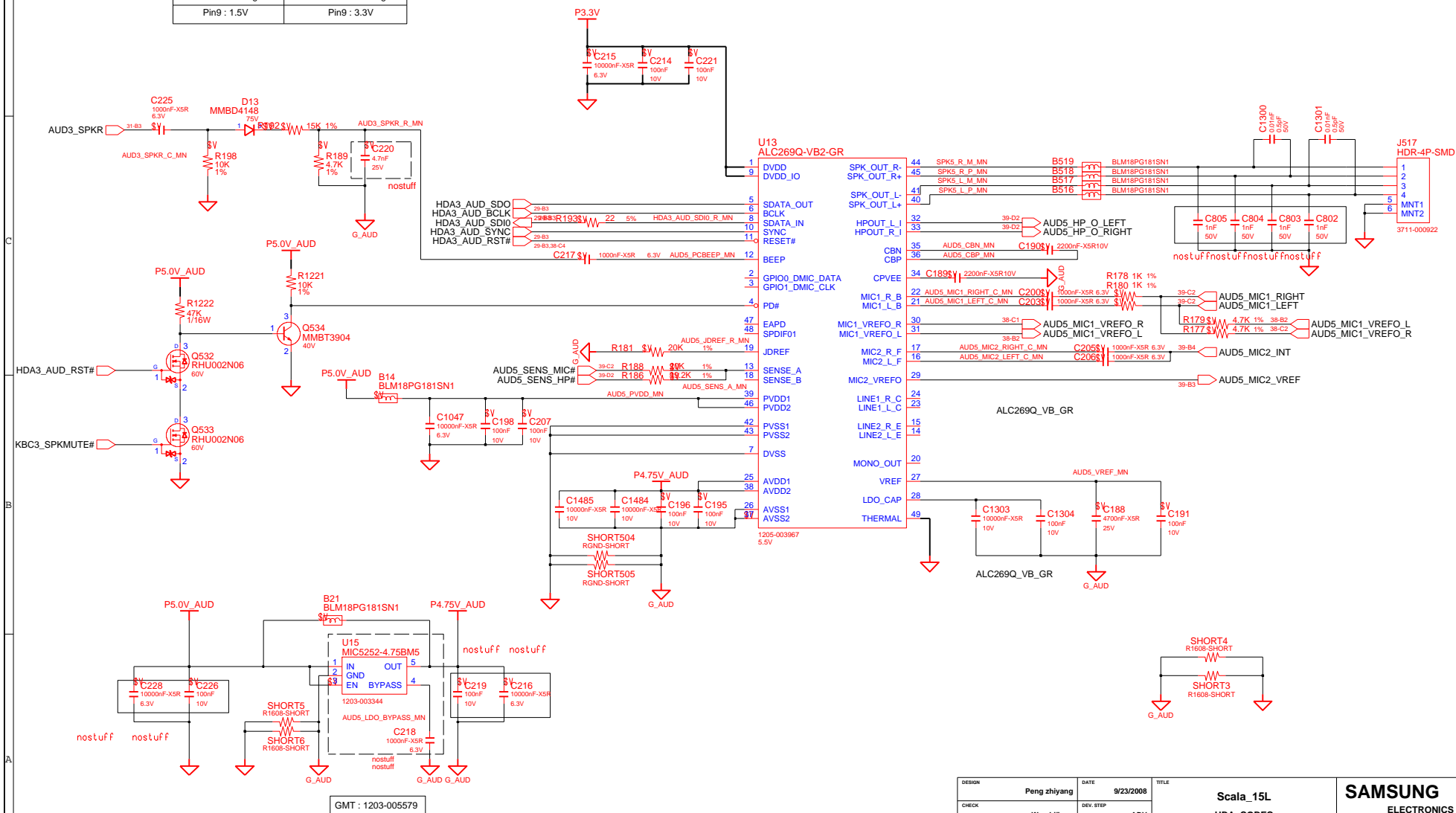



DESIGN	Peng zhiyang	DATE	8/14/2009	TITLE Scala_15L HDMI HDMI Connector	SAMSUNG ELECTRONICS
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APPROVAL	BC Lee	REV	0.1		
MODULE CODE	LAST EDIT				
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				PART NO. BA14-xxxxxA	

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HD AUDIO (ALC269Q)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

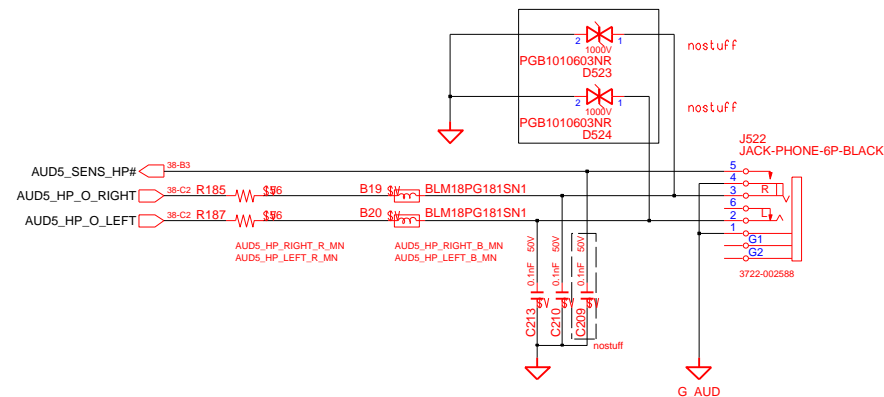


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APPROVAL	BC Lee	REV	0.1		
MODULE CODE					
LAST EDIT				July 14, 2010 20:53:00 PM	PAGE 38 OF 59

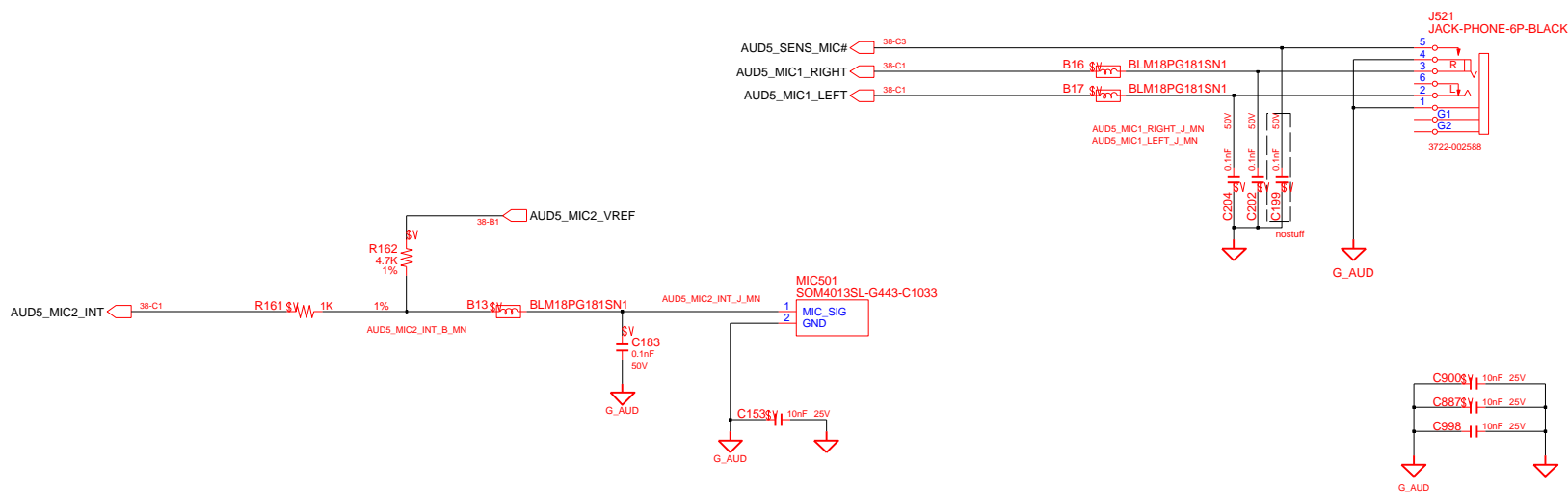
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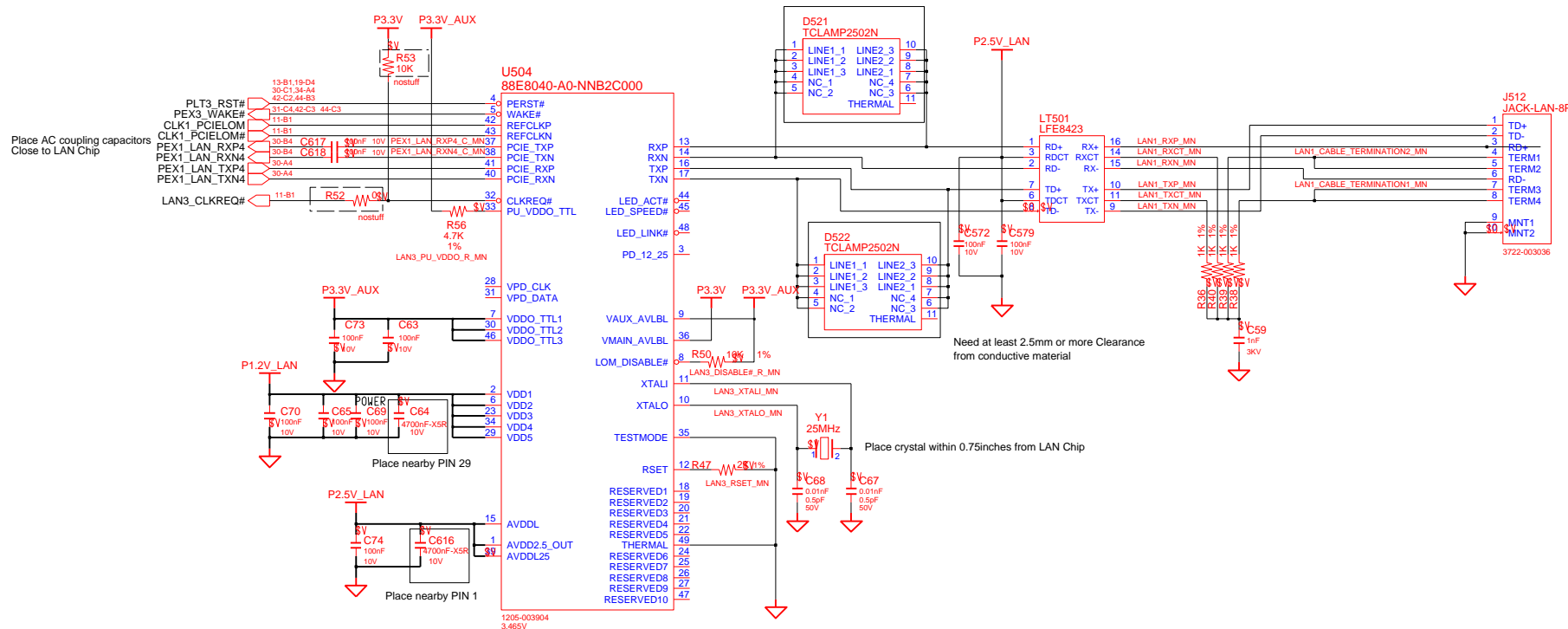
HEADPHONE(BLACK)



MIC JACK(BLACK)



DESIGN	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L	SAMSUNG ELECTRONICS
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APPROVAL	BC Lee	REV	0.1		AUDIO INPUT/OUTPUT	
MODULE CODE		LAST EDIT	July 14, 2010 20:53:00 PM	PAGE	39 OF 59	

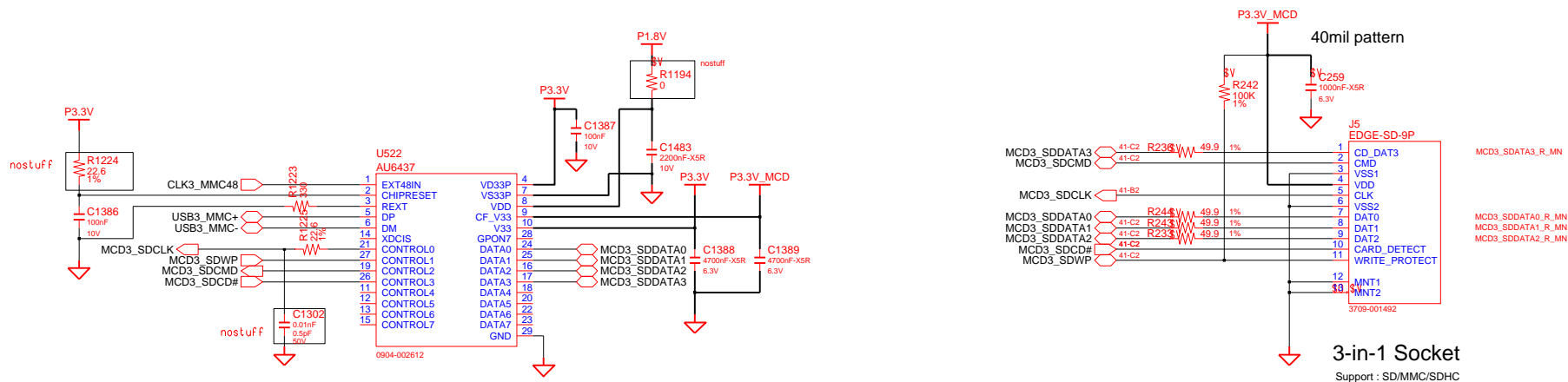


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APPROVAL	BC Lee	REV	0.1			
MODULE CODE			LAST EDIT July 14, 2010 20:53:00 PM			PAGE 40 OF 59

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3 IN 1 CARD (AU6437)



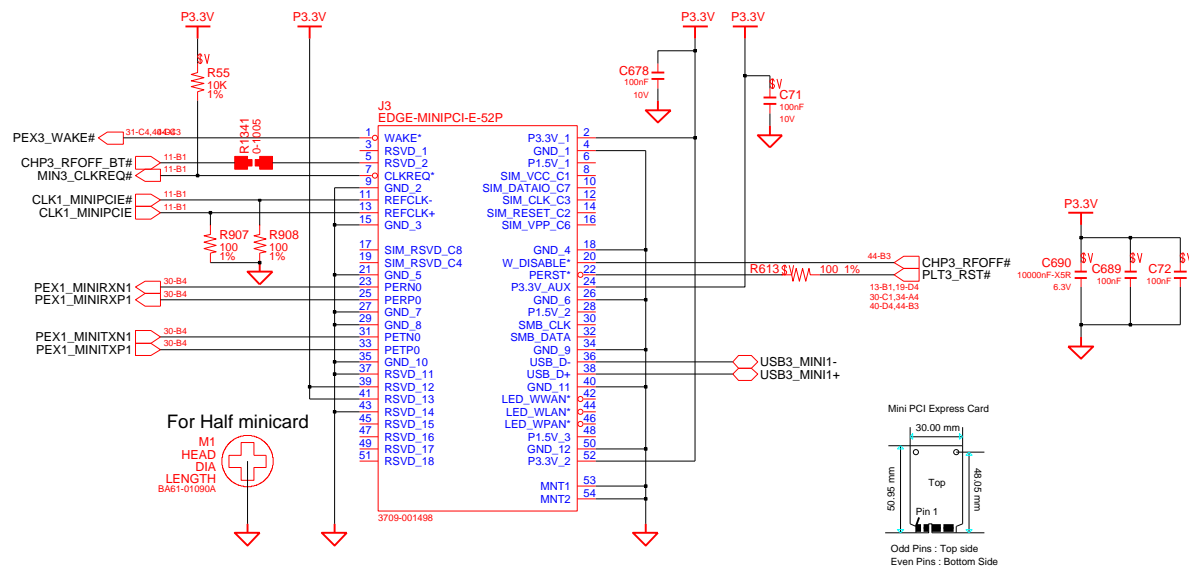
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MODULE CODE		LAST EDIT	July 14, 2010 20:53:00 PM	PAGE	41 OF 59	

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Wireless LAN

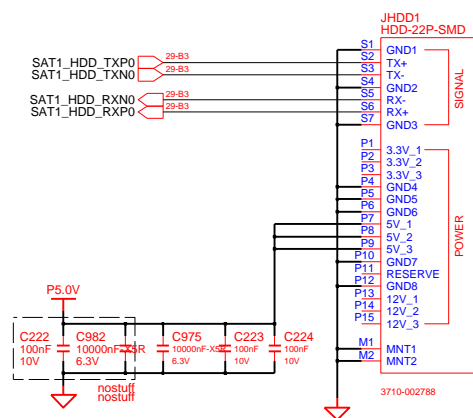
WLAN, 4mm



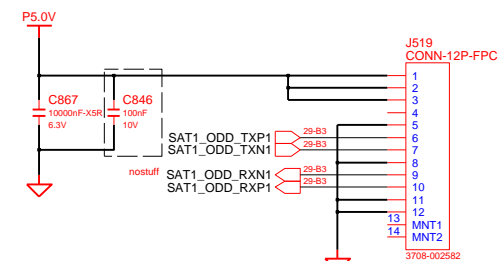
DESIGN	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV		MINI_PCIE_CONN	
APPROVAL	BC Lee	REV	0.1		WLAN & HSDPA & SIM CARD	
MODULE CODE		LAST EDIT	July 14, 2010 20:53:00 PM			
PAGE 42 OF 59						PART NO. BA41-xxxxxA

SATA I/F CONN

SATA HDD CONN



MAIN TO SUB SATA ODD CONN



DESIGN	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV	SATA_DEVICES	PART NO.	
APPROVAL	BC Lee	REV	0.1	HDD & ODD SUB CONNECTOR	BA41-xxxxxA	
MODULE CODE		LAST EDIT	July 14, 2010 20:53:00 PM	PAGE	43 OF 59	

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MICOM_MEC1300

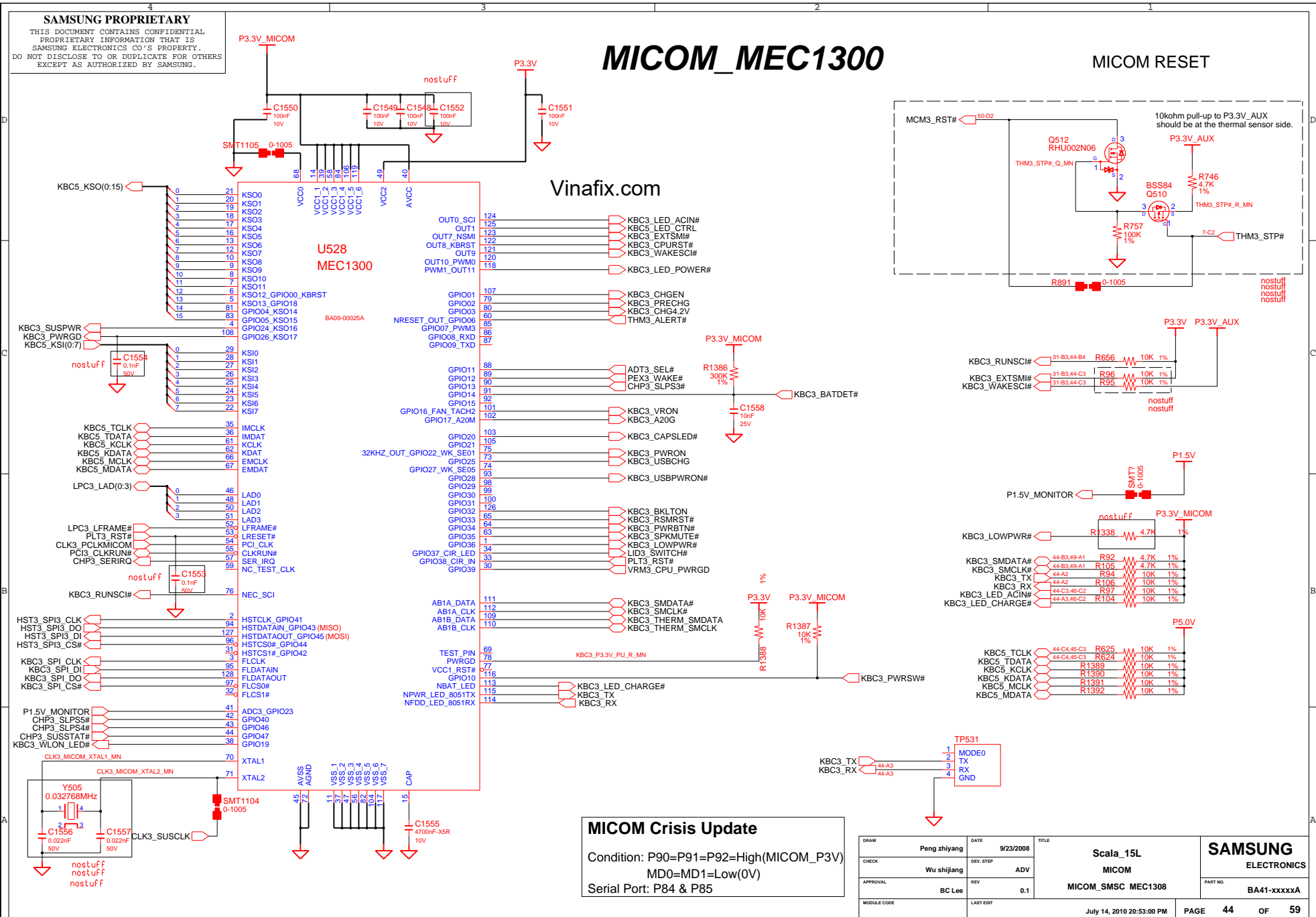
MICOM RESET

Vinafix.com

MICOM Crisis Update

Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

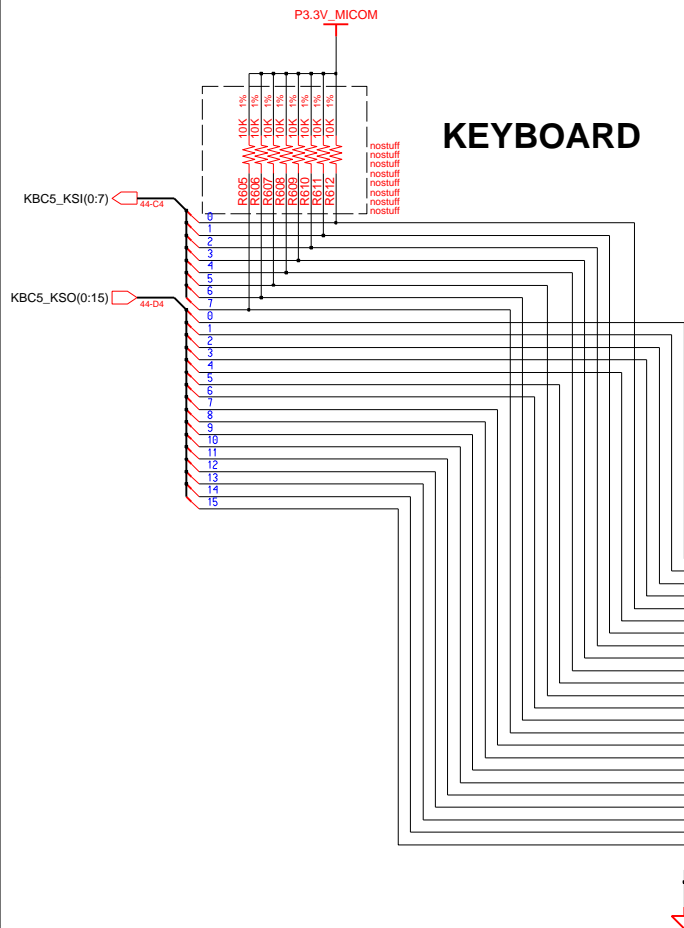
DRAW	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV		MICOM	
APPROVAL	BC Lee	REV	0.1		MICOM_SMSC MEC1308	
MODULE CODE		LAST EDIT			July 14, 2010 20:53:00 PM	PAGE 44 OF 59



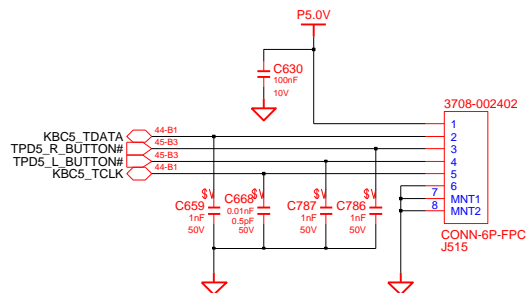
Micom Glue Logic

TOUCHPAD LED

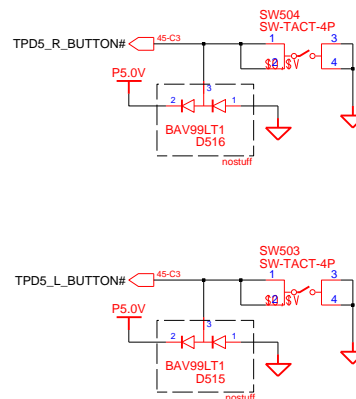
KEYBOARD



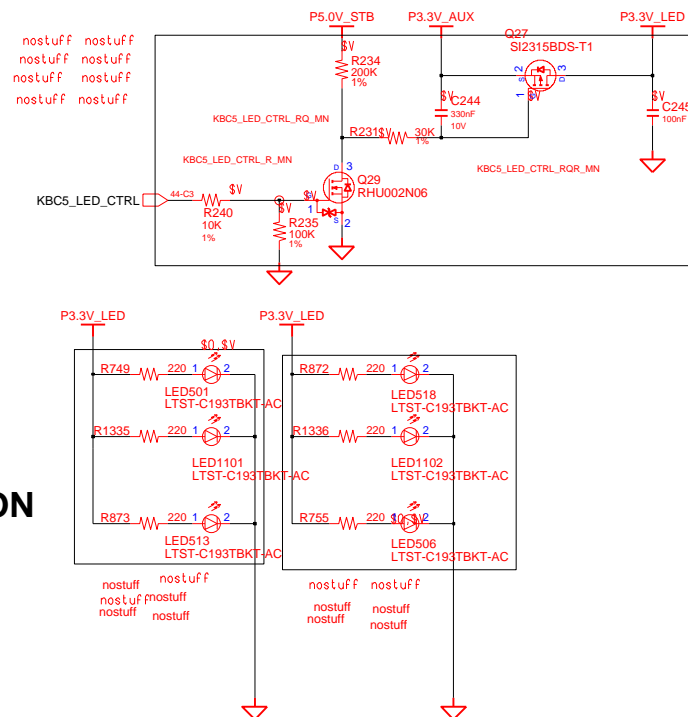
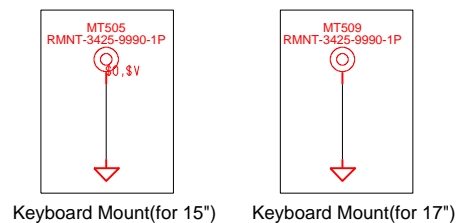
TOUCHPAD



TOUCHPAD BUTTON



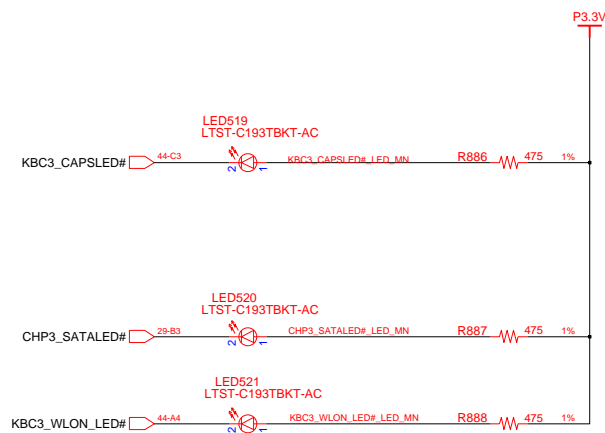
LID SWITCH



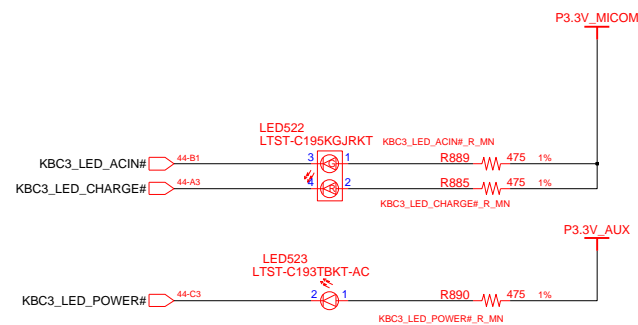
DESIGN	Peng zhiyang	DATE	9/23/2008	TITLE Scala_15L MICOM GLUE LOGIC KETBOARD & TOUCHPAD	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV		
APPROVAL	BC Lee	REV	0.1		
PART NO. BA41-xxxxxxA					
MODULE CODE	LAST EDIT			July 14, 2010 20:53:00 PM	PAGE 45 OF 59


LEDs

FUNCTION KEY LED



ADAPTERIN/CHARGING LED

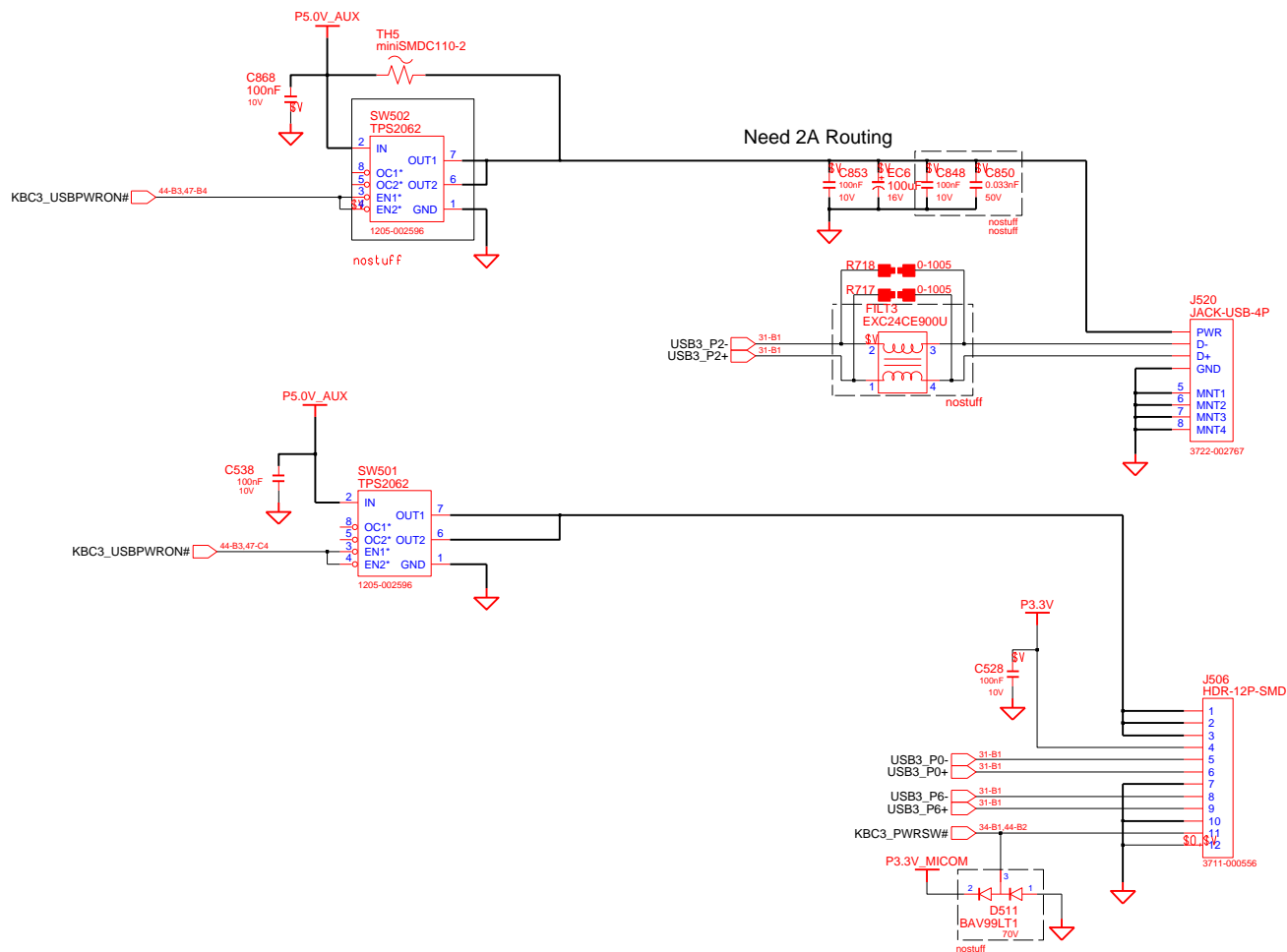


DRAW	Peng zhiyang	DATE	9/23/2008	TITLE Scala_15L LED_SWITCH LED_SWITCH	
CHECK	Wu shijiang	DEV. STEP	ADV		
APPROVAL	BC Lee	REV	0.1		
MODULE CODE	LAST EDIT		July 14, 2010 20:53:00 PM		

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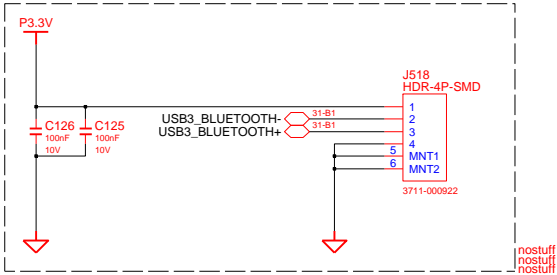
USB Connectors



DESIGN	Peng zhiyang	DATE	9/23/2008	Scala_15L USB_CONN USB & eSATA		SAMSUNG ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	ADV				
APPROVAL	BC Lee	REV	0.1				
MODULE CODE				LAST EDIT		PART NO.	
				July 14, 2010 20:53:00 PM		PAGE	47 OF 59

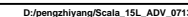
USB I/F Devices

Bluetooth Interface



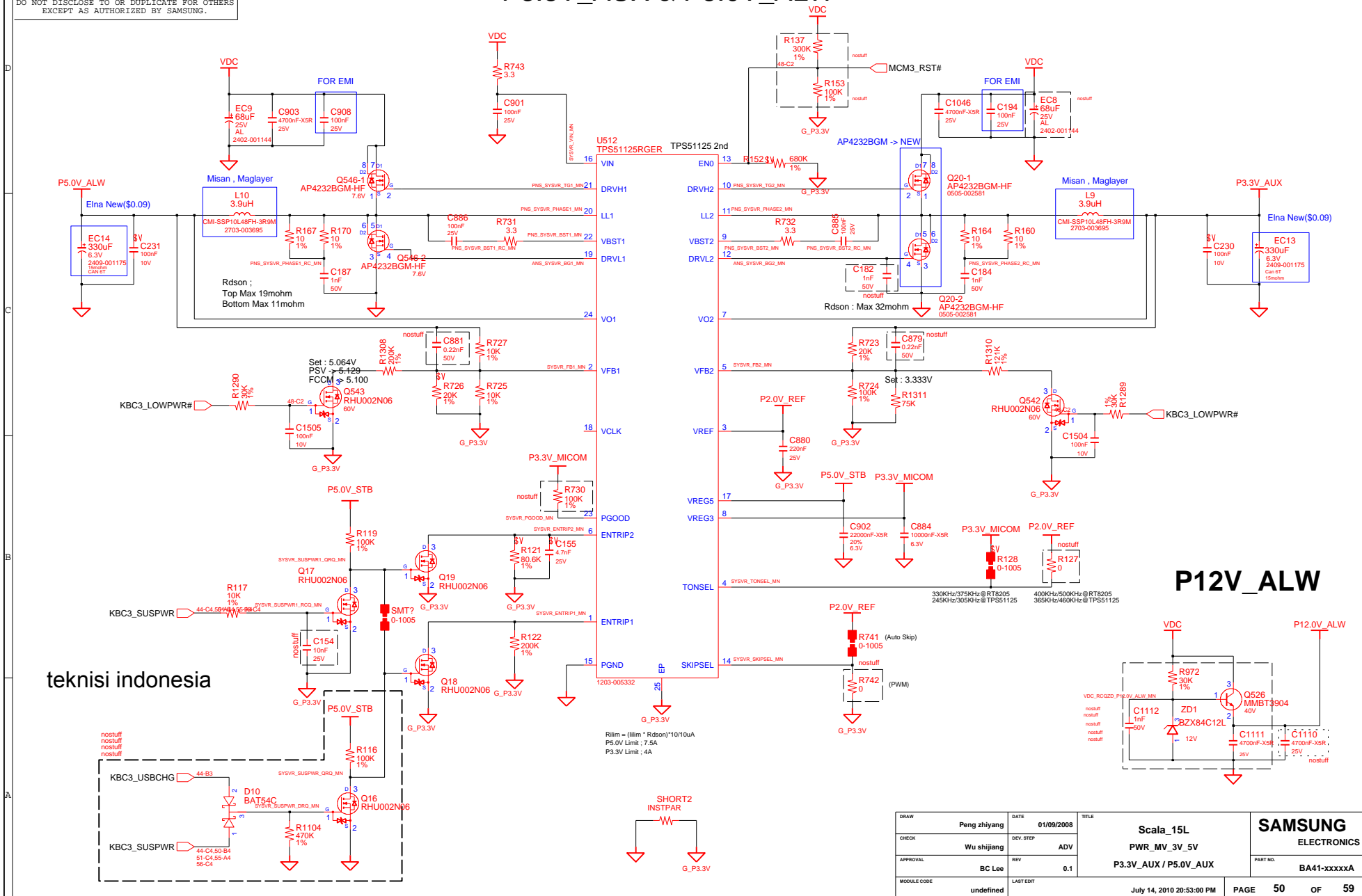
DESIGN	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L	SAMSUNG
CHECK	Wu shijiang	DEV. STEP	ADV	USB_DEVICES	USB_DEVICES	ELECTRONICS
APPROVAL	BC Lee	REV	0.1	BLUETOOTH & CAMERA	PART NO.	BA41-xxxxxA
MODULE CODE	LAST EDIT			July 14, 2010 20:53:00 PM	PAGE	48 OF 59

CHARGE & POWER MANAGEMENT



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P3.3V AUX & P5.0V ALW

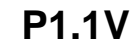


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[illegible]

DRAW	Peng zhiyang	DATE	9/23/2008	TITLE		<div>Scala_15L</div> <div>PWR_MEMORY</div> <div>DDR2 POWER</div>		<div>SAMSUNG</div> <div>ELECTRONICS</div>	
CHECK	Wu shijiang	DEV. STEP	ADV						
APPROVAL	BC Lee	REV	0.1			PART NO.		BA41-XXXXXA	
MODULE CODE		undefined		LAST EDIT		July 14, 2010 20:53:00 PM		PAGE	51 OF 59

CHIPSET POWER (P1.05V)



D:/pengzhiyang/Scala_15L_ADV_0713

M92_S2_GFX3_VOLTID

G1	G0	
1	1	0.90V (0.902V)
1	0	1.00V (1.006V)
0	1	1.10V (1.111V)
0	0	1.20V (1.202V)

Park_S3_GFX3_VOLTID

G1	G0	
1	1	0.90V (0.902V)
1	0	1.00V (1.006V)
0	1	1.10V (1.111V)
0	0	1.20V (1.202V)

For M92-S2

	For M92-S2	For Park-S3
RSET2	22K, 2007-007311	30.1K, 2007-008359
RSET3	30K, 2007-008275	15K, 2007-007132
RSET4	22K, 2007-007311	30K, 2007-008275

M92_S2_GFX3_VOLT		
G1	G0	
1	1	0.90V (0.902V)
1	0	1.00V (1.006V)
0	1	1.10V (1.111V)
0	0	1.20V (1.202V)

G1	G0	
1	1	0.90V (0.903V)
1	0	0.95V (0.955V)
0	1	1.00V (1.003V)
0	0	1.10V (1.116V)

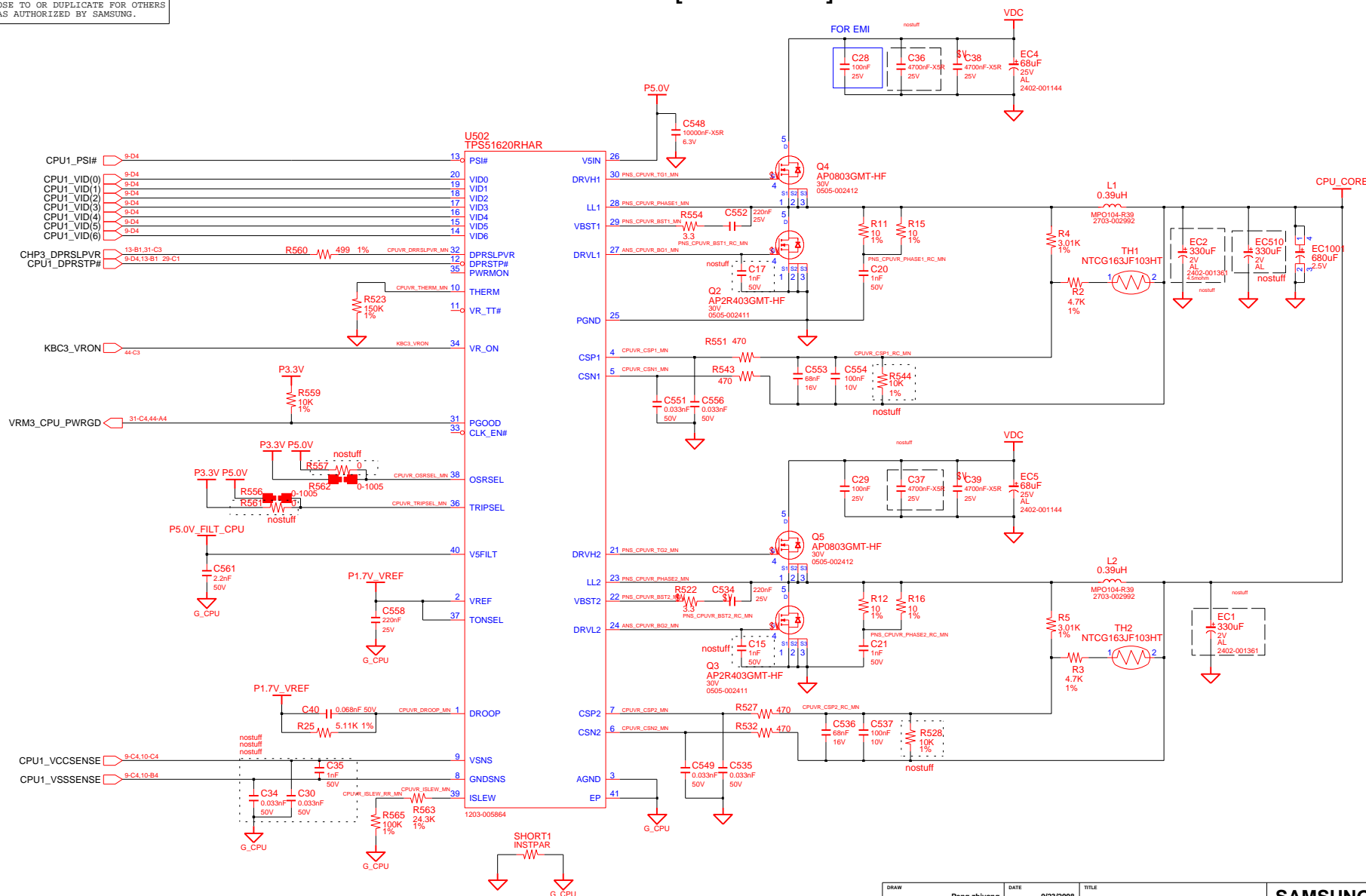
	For M92-S2	For Park-S3
RSET2	22K, 2007-007311	30.1K, 2007-008333
RSET3	30K, 2007-008275	15K, 2007-007132
RSET4	22K, 2007-007311	30K, 2007-008275

DESIGN	Peng zhiyang	DATE	9/3/2009	TITLE Scala_15L PWR_MV_Cantiga EGFX CORE	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	ADV		
APPROVAL	BC Lee	REV	0.1		
MODULE CODE	LAST EDIT				
				July 14, 2010 20:53:00 PM	PAGE 53 OF 59

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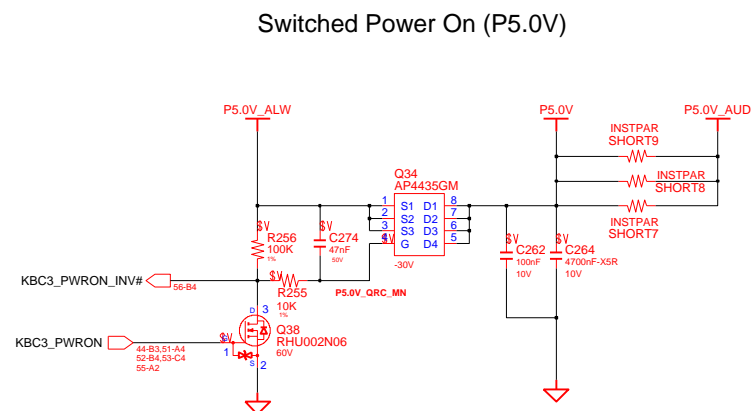
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CPU VRM [TI IMVP6+]

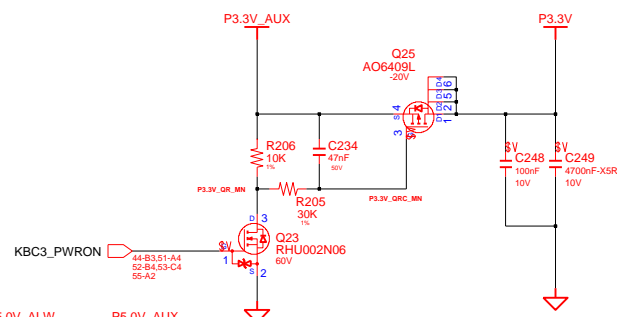


DRAW	Peng zhiyang	DATE	9/23/2008	TITLE	Scala_15L
CHECK	Wu shijiang	DEV. STEP	ADV		PWR_CPU_MV_TPS51620
APPROVAL	BC Lee	REV	0.1		CPU1 VRM (IMVP6+)
MODULE CODE	undefined	LAST EDIT	July 14, 2010 20:53:00 PM	PAGE	54 OF 59
					SAMSUNG ELECTRONICS
					PART NO. BA41-xxxxxA

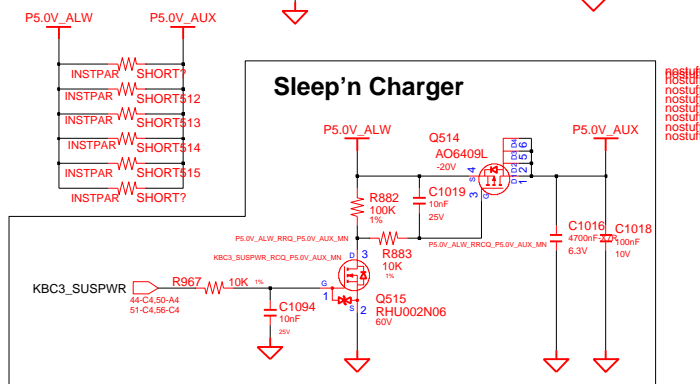
Multi @ SI4435DDY



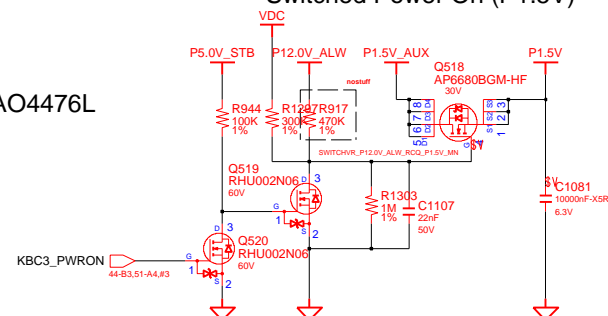
Switched Power On (P3.3V)



Sleep'n Charger



Switched Power On (P1.5V)



Multi @ AO4476L

Multi @ AP2607GY

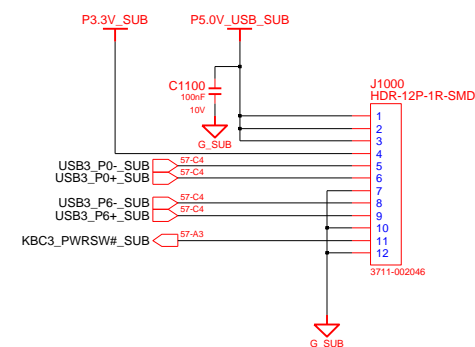
DRAW	Peng zhiyang	DATE	9/23/2008	TITLE Scala_15L PWR_MY_SWITCHED SWITCHED POWER	SAMSUNG ELECTRONICS	
CHECK	Wu shijiang	REV. STEP	ADV			
APPROVAL	BC Lee	REV	0.1		PART NO.	BA41-xxxxxA
MODULE CODE	LAST EDIT				July 14, 2010 20:53:00 PM	PAGE 55

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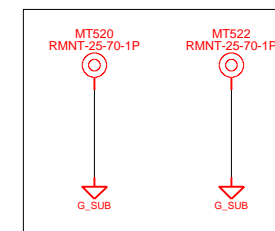
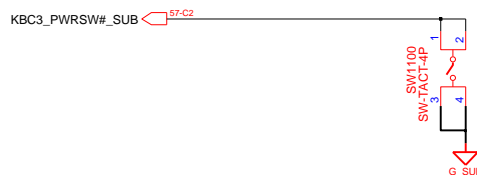
DRAW	Peng zhiyang	DATE	9/23/2008	Scala_15L PWR_MV_DISCHARGER DISCHARGING LOGIC	SAMSUNG ELECTRONICS		
CHECK	Wu shijiang	DES. STEP	ADV		PART NO. BA41-xxxxxA		
APPROVAL	BC Lee	REV	0.1				
MODULE CODE	undefined	LAST EDIT	July 14, 2010 20:53:00 PM			PAGE	56

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SUB TO MAIN USB CONN



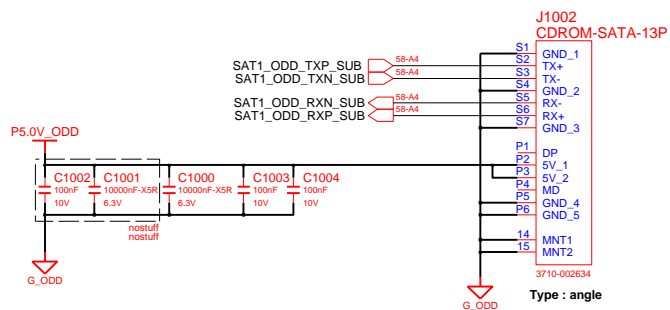
Power Button



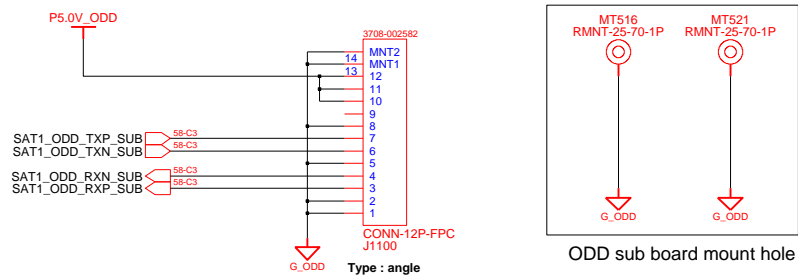
USB sub board mount hole

DESIGN		Peng zhiyang		DATE	8/22/2009		TITLE Scala_15L SUB BOARD1 USB PORT, POWER SW SUBBOARD		SAMSUNG ELECTRONICS		
CHECK		Wu shijiang		DEV. STEP	ADV				PART NO.		
APPROVAL		BC Lee		REV	0.1				BA41-xxxxxxA		
MODULE CODE				LAST EDIT		July 14, 2010 20:53:00 PM			PAGE 57 OF 59		

SATA ODD CONN



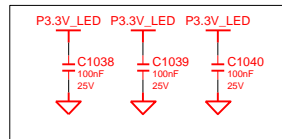
SUB TO MAIN SATA ODD CONN



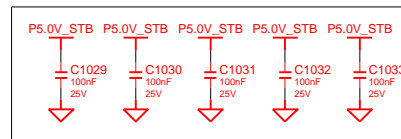
DRAW	Peng zhiyang	DATE	9/23/2008	TITLE Scala_15L SUB BOARD2 SATA ODD SUB BOARD	SAMSUNG ELECTRONICS		
CHECK	Wu shijiang	DES. STEP	ADV				
APPROVAL	BC Lee	REV	0.1		PART NO.	BA41-xxxxxxA	
MODULE CODE	undefined	LAST EDIT	July 14, 2010 20:53:00 PM		PAGE	58	OF 59

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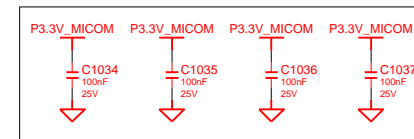
(30,90) x 7, (25,70) x 1



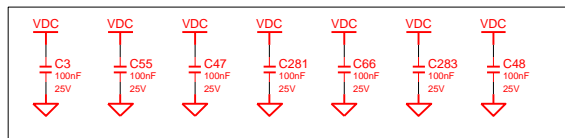
Add for EMC, 2009.09.11



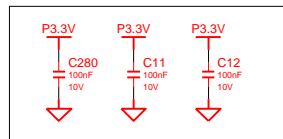
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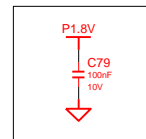
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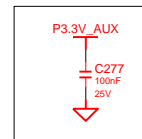
Add for EMC, 2009.09.10



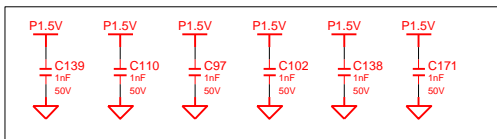
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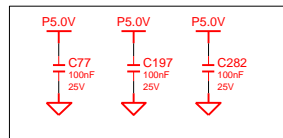
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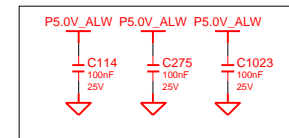
Add for EMC, 2009.09.10



Add for EMC (Stitching), 2009.09.10



Add for EMC, 2009.09.10



Add for EMC, 2009.09.10

DRAW	Peng zhiyang	DATE	9/23/2008	Scala_15L ETC EMC CAP & MT HALL		SAMSUNG ELECTRONICS			
CHECK	Wu shijiang	DEV. STEP	ADV						
APPROVAL	BC Lee	REV	0.1						
MODULE CODE		LAST EDIT		July 14, 2010 20:53:00 PM		PAGE	59	OF	59